SPECTRUM
INSTRUMENTATION

MX.72xx - 16 bit Digital Pattern Generator with programmable logic levels

- **PXI 3U / CompactPCI 3U format**
- **Programmable output levels from -2,0 V up to +10,0 V**
- **Levels individually programmable per 4 bit**
- **Up to 40 MS/s at 16 bit**
- **Possible use of memory saving 8 bit mode**
- **All Outputs can be separately disabled (Tristate)**
- **Hardware controlled differential output possible (8 bit)**
- **Up to 128 MByte memory**
- **Output in FIFO mode**
- **Synchronization possible**

Product range overview

| Model	8 bit	16 bit
MX.7210	10 MS/s	10 MS/s
MX.7220	40 MS/s	40 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows NT/2000 32 bit drivers
- Windows XP/Vista/7/8/10, 32 and 64 bit driver
- Linux 32bit and 64bit drivers
- SBench 6.x Base version for Windows and Linux
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic & Excel examples
- Python examples
- LabWindows/CVI examples
- LabVIEW - drivers and examples
- MATLAB - drivers and examples
- Other 3rd party drivers (e.g. VEE,DASYLab) are partly available upon request

General Information

The MX.72xx pattern generator series gives the user the possibility to generate digital data with a wide range of output levels. For every 4 bit the LOW and HIGH levels can be programmed from -2.0 V up to +10.0 V. Even at high speeds you are not limited concerning the maximum output swing. This enables the user to drive devices of nearly any logic family, like ECL, PECL, TTL, LVDS, LVTTL, CMOS or LVCMOS. The potentially necessary differential signals are generated in hardware, so that only one data bit is used for each pair of differential signals. All outputs can be seperately disabled allowing the easy connection with digital acquisition boards and the adaption to a wide range of test setups. The internal standard synchronisation bus allows synchronisation of several MX.xxxx boards. Therefore the MX.72xx board can be used as an enlargement to any digital or analog board.

Hardware block diagram
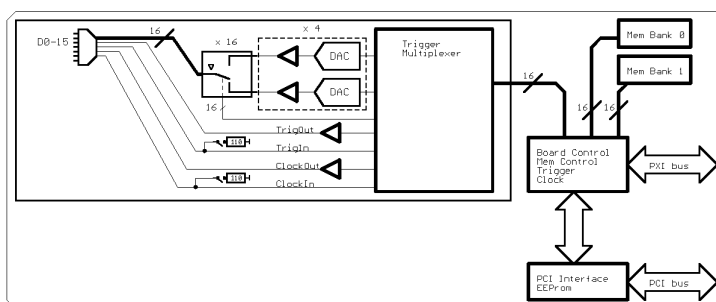
Software programmable parameters

sampling rate	1 kS/s to max sampling rate, external clock, ref clock, PXI clock
Output level	LOW/HIGH level p. nibble;-2,0 V up to +10,0 V in steps of 1mV
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Data Enable mask	programmable for every single bit
Trigger mode	External TTL, software, PXI Line[5..0], PXI Startrigger
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

Semiconductor test	Production test	Burn-in test
Laboratory purposes	Pattern generator	Semiconductor development
Process control	ATE	

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is posible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software commend one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

External trigger I/O

All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock
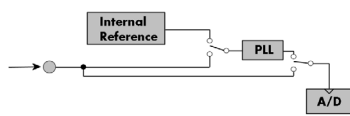
The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.
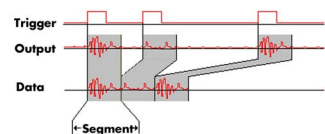
ECL Mode
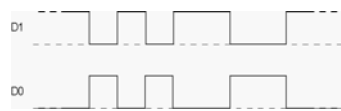
When the ECL mode is activated, differential signals wich are needed for e.g. ECL interfacing are generated in hardware on the odd data outputs. This results in the use of only one data bit for every pair of differential outputs and allows a very efficiently use of memory.

Multiple Replay

The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

Gated Replay
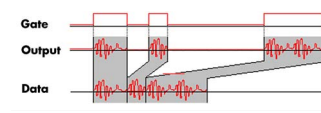
The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a programmed level.

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Continuous output

When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

Technical Data

Internal samplerate	1 kS/s up to maximum (depending on model)			Dimension	160 mm x 100 mm (Standard 3U)	
External samplerate	DC up to maximum (depending on model)			Width (MX.7210)	1 slot	
Clock input impedance	110 Ohm / 50 kOhm || 15 pF			Width (MX.7220)	2 slots	
Trigger input impedance	110 Ohm / 50 kOhm || 15 pF					
Output impedance	approximately 80 Ohm			Output connector	40 pole half pitch (Hirose FX2 series)	
Data signal level	programmable from -2.0 V up to +10.0 V with an accuracy of ±10 mV			Power connector (MX.7220 only)	soldered Y - cable with Molex 8981 (5,25" disc drive connector)	
Output swing	0.1 … 12.0 V					

	per pin	per nibble	per card	Operating temperature	0°C to 50°C
Maximum output current	100 mA	200 mA	0.5 A (MX.7210 only)	Storage temperature	-10°C to 70°C
	1 MHz	40 MHz		Humidity	10% to 90%
Rise time[a]	2.00 ns	2.25 ns		MTBF	100000 hours
Fall time[a]	2.00 ns	2.25 ns			

Multi: Trigger to 1st sample delay	fixed
Multi: Recovery time	< 20 samples (16 - 32 bit)

	32 bit	16 bit	8 bit
Trigger accuracy (samples)	1	1	2

a. Tested with full output swing from -2.0 V to 10.0 V with no load

Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Power consumption (maximum value)			Full speed	
	+3.3 V (PXI Bus)	+5 V (PXI Bus)	+12 V (PXI Bus)	+12 V (Connector)
MX.7210 (16 bit output @ 10 MS/s)[a]	0.76 A (2.5 W)	0.5 A (2.5 W)	0.35 A (4.2 W)	–
MX.7220 (16 bit output @ 40 MS/s)[b]	0.91 A (3.0 W)	0.6 A (3.0 W)	0 A	1.8 A (21.6 W)

a. Tested with full output swing from -2.0 to 10.0 V with no load
b. Tested with full output swing from -2.0 V to 10.0 V with 50 mA output current per pin

Order Informations

The card is delivered with 64 MByte on-board memory and supports standard mode (Scope), FIFO mode (streaming), Multiple Recording/Replay and Gated Sampling/Replay. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows), LabWindows/CVI, Delphi, Visual Basic, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASYLab may be available on request.

One digital connecting cable Cab-d40-idc-100 is included in the delivery for every digital connection (each 16 channels).

Versions

Order no.	8 Bit	16 Bit
MX.7210	10 MS/	10 MS/s
MX.7220	40 MS/s	40 MS/s

Memory

Order no.	Option
MX.7xxx-128M	Memory upgrade to 128 MB of total memory
MX.7xxx-up	Additional fee for later memory upgrade

Cable

Order no.	Option
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to 2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

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