

M4i.22xx-x8 - 8 bit Digitizer up to 5 GS/s

- 5 GS/s on one channel
- 2.5 GS/s on two channels
- 1.25 GS/s on four channels
- up to 1.5 GHz bandwidth
- Ultra Fast PCI Express x8 Gen 2 interface
- Simultaneously sampling on all channels
- 4 input ranges: ±200 mV up to ±2.5 V
- Low voltage input range option ±40 mV up to ±500 mV
- Programmable input offset of ±200%
- 4 GSample on-board memory
- Window, re-arm, OR/AND trigger
- Synchronization of up to 8 cards per system
- Features: Single-Shot, Streaming, Multiple Recording, Gated Sampling, ABA, Timestamps
- Direct data transfer to CUDA GPU using SCAPP optio





- Block Average up to 128k
- Block Statistics/Peak Detect





- PCle x8 Gen 2 Interface
- Works with x8/x16* PCle slots
- Sustained streaming mode more than 3.4 GB/s**



Operating Systems

- Windows 7 (SP1), 8, 10
- Linux Kernel 2.6, 3.x, 4.x
- Windows/Linux 32 and 64 bit

Recommended Software

- Visual Basic, Visual C++, C++ Builder, GNU C++, Delphi, VB.NET, C#, J#, Java, Python
- SBench 6

Drivers

- MATLAB
- LabVIEW
- LabWindows/CVI
- IVI

Model	Bandwidth	1 channel	2 channels	4 channels
M4i.2234-x8	1.5 GHz	5 GS/s	2.5 GS/s	1.25 GS/s
M4i.2233-x8	1.5 GHz	5 GS/s	2.5 GS/s	
M4i.2230-x8	1.5 GHz	5 GS/s		
M4i.2221-x8	1.5 GHz	2.5 GS/s	2.5 GS/s	
M4i.2223-x8	1.5 GHz	2.5 GS/s	1.25 GS/s	
M4i.2220-x8	1.5 GHz	2.5 GS/s		
M4i.2212-x8	500 MHz	1.25 GS/s	1.25 GS/s	1.25 GS/s
M4i.2211-x8	500 MHz	1.25 GS/s	1.25 GS/s	
M4i.2210-x8	500 MHz	1.25 GS/s		

General Information

The M4i.22xx-x8 series digitizers deliver the highest performance in both speed and resolution. The series includes PCle cards with either one, two or four synchronous channels. The ADCs can sample at rates from 1.25 GS/s up to 5 GS/s with a maximum bandwidth of up to 1.5 GHz.

The digitizers feature a PCI Express x8 Gen 2 interface that offers outstanding data streaming performance. The interface and Spectrums optimized drivers enable data transfer rates in excess of 3.4 GB/s so that signals can be acquired, stored and analyzed at the fastest speeds. The cards are still software compatible with the drivers from earlier Spectrum digitizers starting with M2i series.

^{*}Some x16 PCIe slots are for the use of graphic cards only and can'tbe used for other cards. **Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

Software Support

Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, LabWindows/CVI, Delphi, Visual Basic, VB.NET, C#, J#, Python, Java and IVI are included.

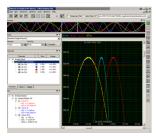
Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++,

Python as well as the possibility to get the driver sources for your own compilation.

SBench 6



A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial

setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW, MATLAB or LabWindows/CVI. All drivers come with detailed documentation and working examples are included in the delivery. Support for other software packages, like VEE or DasyLab, can also be provided on request.

SCAPP - CUDA GPU based data processing



For applications requiring high powered signal and data processing Spectrum offers SCAPP (Spectrum's CUDA Access for Parallel Processing). The SCAPP SDK allows a direct link between Spectrum digitizers and CUDA based GPU cards. Once in the

GPU users can harness the processing power of the GPU's multiple (up to 5000) processing cores and large (up to 24 GB) memories. SCAPP uses an RDMA (Linux only) process to send data at the digitizers full PCle transfer speed to the GPU card. The SDK includes a set of examples for interaction between the digitizer and the GPU

card and another set of CUDA parallel processing examples with easy building blocks for basic functions like filtering, averaging, data de-multiplexing, data conversion or FFT. All the software is based on C/C++ and can easily be implemented, expanded and modified with normal programming skills.

Hardware features and options

PCI Express x8



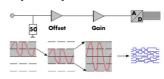
The M4i series cards use a PCI Express x8 Gen 2 connection. They can be used in PCI Express x8 and x16 slots with Gen 1, Gen 2 or Gen 3. The maximum sustained data transfer rate is more than 3.3

GByte/s (read direction) or 2.8 GByte/s (write direction) per slot. Server motherboards often recognize PCI Express x4 connections in x8 slots. These slots can also be used with the M4i series cards but with reduced data transfer rates.

Connections

- The cards are equipped with SMA connectors for the analog signals as well as for the external trigger and clock input. In addition, there are five MMCX connectors that are used for an additional trigger input, a clock output and three multi-function I/O connectors. These multi-function connectors can be individually programmed to perform different functions:
- Trigger output
- Status output (armed, triggered, ready, ...)
- Synchronous digital inputs, being stored inside the analog data samples
- Asynchronous I/O lines

Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands one can select a matching input

range and the signal offset can be compensated by programmable AC coupling or offset shifting.

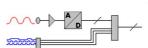
Software selectable lowpass filter

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be useful especially with low voltage input signals.

Automatic on-board calibration

Every channel of each card is calibrated in the factory before the board is shipped. However, to compensate for environmental variations like PC power supply, temperature and aging the software driver includes routines for automatic offset and gain calibration. This calibration is performed on all input ranges of the "Buffered" path and uses a high precision onboard calibration reference.

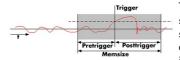
Digital inputs



This option acquires additional synchronous digital channels phasestable with the analog data. As default a maximum of 3 additional

digital inputs are available on the front plate of the card using the multi-purpose I/O lines.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a

trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO or streaming mode is designed for continuous data transfer between the digitizer card and the PC memory. When mounted in a PCI Express x8 Gen 2 interface read streaming speeds of up to 3.4 GByte/s are possible. The control of the data stream is done automatically by the driver on interrupt request basis. The complete installed onboard memory is used to buffer the data, making the continuous streaming process extremely reliable.

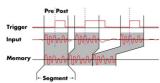
Channel trigger

The digitizers offer a wide variety of trigger modes. These include a standard triggering mode based on a signals level and slope, like that found in most oscilloscopes. It is also possible to define a window mode, with two trigger levels, that enables triggering when signals enter or exit the window. Each input has its own trigger circuit which can be used to setup conditional triggers based on logical AND/OR patterns. All trigger modes can be combined with a re-arming mode for accurate trigger recognition even on noisy signals.

External trigger input

All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

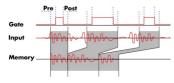
Multiple Recording



The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in be-

tween. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

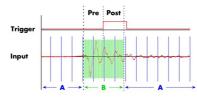
Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start

of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

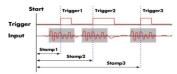
ABA mode



The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact

position of the trigger events is stored as timestamps in an extra memory.

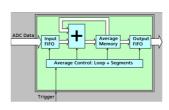
Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, ex-

ternally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

Firmware Option Block Average

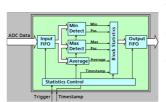


The Block Average Module improves the fidelity of noisy repetitive signals. Multiple repetitive acquisitions with very small dead-time are accumulated and averaged. Random noise is reduced by the averaging process improving

the visibility of the repetitive signal. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

Firmware Option Block Statistics (Peak Detect)



The Block Statistics and Peak Detect Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for minimum and maximum peak and a summary including minimum, maximum, aver-

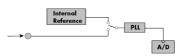
age, timestamps and position information is stored in memory. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

External clock input and output

Using a dedicated connector a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock on a separate connector to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality

measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this

way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub



The Star-Hub is an additional module allowing the phase stable synchronization of up to 8 boards of a kind in one system. Independent of the number of boards there is no phase delay between all channels. The Star-Hub distributes trigger and clock information between all boards to ensure all connected boards are running with the same clock and trigger. All trigger

sources can be combined with a logical OR allowing all channels of all cards to be the trigger source at the same time.

External Amplifiers



For the acquisition of extremely small voltage levels with a high bandwidth a series of external amplifiers is available. Each of the one channel amplifiers is working with a fixed input impedance and allowsdepending on the bandwidth to select different amplification levels between x10 (20 dB) up to x1000 (60 dB). Us-

ing the external amplifiers of the SPA series voltage levels in the uV and mV area can be acquired.

Technical Data

Analog Inputs

Resolution 8 Rit Single-ended Input Type ADC Differential non linearity (DNL) ±0.35 LSB ADC only ADC Integral non linearity (INL) ADC only ±0.9 LSB

sampling rate 1.25 GS/s 10-16 ADC Bit Error Rate (BER)

software programmable Channel selection 1, 2, or 4 (maximum is model dependent)

Analog Input impedance fixed 50 Ω

 ± 200 mV, ± 500 mV, ± 1 V, ± 2.5 V (programmable input offset at 0%) Input Ranges (standard ranges) software programmable Input Ranges (Low Voltage Option) software programmable ±40 mV, ±100 mV, ±200 mV, ±500 mV (programmable input offset at 0%)

Programmable Input Offset software programmable ±200% (allowing bi-polar ranges to become uni-polar)

Input Coupling software programmable AC/DC Max DC voltage if AC coupling active +30 V

< 0.5 LSB Offset error (full speed) after warm-up and calibration Gain error (full speed) after warm-up and calibration < 2.0 LSB

Crosstalk 20 MHz sine signal (standard ranges) ≥ ±500 mV standard range < -96 dB (all channel same input range) = ±200 mV standard range < -88 dB (all channel same input range) Crosstalk 20 MHz sine signal (standard ranges) $\geq \pm 500$ mV standard range < -78 dB (all channel same input range) Crosstalk 100 MHz sine signal (standard ranges) Crosstalk 100 MHz sine signal (standard ranges) = ±200 mV standard range < -65 dB (all channel same input range)

Over voltage protection input range (standard ranges) ±200 mV ±500 mV ±1 V input range (low voltage option) ±40 mV ±100 mV ±200 mV ±500 mV 22.5 dBm 27 0 dBm 27 0 dBm

max. continuous input power 27.0 dBm max. peak input voltage ±3 V ±7.5 V ±15 V ±30 V

<u>Trigger</u>

Available trigger modes software programmable Channel Trigger, External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)

1 engine per channel with two individual levels, 2 external triggers

Channel trigger level resolution software programmable

Trigger engines

software programmable Rising edge, falling edge or both edges Trigger edge

0 to (8GSamples - 32) = 8589934560 Samples in steps of 32 samples Trigger delay software programmable

Multi, ABA, Gate: re-arming time 1.25 GS/s or below 80 samples (+ programmed pretrigger) 160 samples (+ programmed pretrigger) 5 GS/s 320 samples (+ programmed pretrigger)

Pretrigger at Multi, ABA, Gate, FIFO software programmable 32 up to 8192 Samples in steps of 3232 up to 16G samples in steps of 32 (defining pretrigger in standard scope mode) Posttrigger software programmable

Memory depth software programmable 64 up to [installed memory / number of active channels] samples in steps of 32 Multiple Recording/ABA segment size 64 up to [installed memory / 2 / active channels] samples in steps of 32 software programmable

Trigger accuracy (all sources) 1 sample

External trigger Ext0 Ext1 External trigger impedance software programmable $50 \Omega / 1 k\Omega$ $1 k\Omega$

External trigger coupling software programmable AC or DC fixed DC External trigger type Window comparator Single level comparator

±10 V External input level $\pm 10 \text{ V} (1 \text{ k}\Omega), \pm 2.5 \text{ V} (50 \Omega).$ 2.5% of full scale range 2.5% of full scale range = 0.5 V

External trigger sensitivity (minimum required signal swing) ±10 V in steps of 1 mV ±10 V in steps of 1 mV External trigger level software programmable

External trigger maximum voltage ±30V ±30 V External trigger bandwidth DC 50 Ω

DC to 200 MHz DC to 150 MHz n.a. DC to 200 MHz 1 kΩ External trigger bandwidth AC 50 Ω 20 kHz to 200 MHz n.a. Minimum external trigger pulse width ≥ 2 samples ≥ 2 samples

Clock

Clack Modes internal PLL, external reference clock, Star-Hub sync (M4i only), PXI Reference Clock (M4x only) software programmable

Internal clock accuracy

divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 262144 Internal clock setup granularity External reference clock range \geq 10 MHz and \leq 1.25 GHz software programmable

External reference clock input impedance 50 O fixed External reference clock input coupling AC coupling

External reference clock input edge Rising edge External reference clock input type Single-ended, sine wave or square wave External reference clock input swing 0.3 V peak-peak up to 3.0 V peak-peak External reference clock input max DC voltage ±30 V (with max 3.0 V difference between low and high level)

External reference clock input duty cycle requirement Clock setup granularity when using reference clock divider: maximum sampling rate divided by: 1, 2, 4, 8, 16, ... up to 262144

Internal reference clock output type Single-ended, 3.3V LVPECL 2.5 GHz / 64 = 39.0625 MHz Internal reference clock output frequency

Star-Hub synchronization clock modes software selectable Internal clock (standard clock mode only), External reference clock

16 up to (128k - 16) in steps of 16 ABA mode clock divider for slow clock software programmable

Channel to channel skew on one card < 60 ps (typical)

< 130 ps (typical, preliminary) Skew between star-hub synchronized cards

	M4i.223x DN2.223-xx DN2.225-xx DN6.225-xx	M4i.222x DN2.222-xx	M4i.221x DN2.221-xx DN6.221-xx	All versions
Input Ranges	Standard Ranges	Standard Ranges	Standard Ranges	Low Voltage Ranges
ADC Resolution	8 bit	8 bit	8 bit	8 bit
max sampling clock	5 GS/s	2.5 GS/s	1.25 GS/s	model dependant
min sampling clock	4.768 kS/s	4.768 kS/s	4.768 kS/s	4.768 kS/s
lower bandwidth limit (DC coupling)	0 Hz	0 Hz	0 Hz	0 Hz
lower bandwidth limit (AC coupling)	< 30 kHz	< 30 kHz	< 30 kHz	< 30 kHz
-3 dB bandwidth (no filter active)	1.5 GHz	1.5 GHz	500 MHz-	700 MHz-
-3 dB bandwidth (BW filter active)	~400 MHz	~400 MHz	~370 MHz	~380 MHz

Block Average Signal Processing Option M4i.22xx/DN2.22x/DN6.22x Series

		Firmware ≥ V1.14	(August 2015)	Firmware < V1.14
Data Mode	software programmable	32 bit mode	16 bit mode	32 bit mode only
Minimum Waveform Length		64 samples	128 samples	64 samples
Minimum Waveform Stepsize		32 samples	64 samples	32 samples
Maximum Waveform Length	1 channel active	64 kSamples	128 kSamples	32 kSamples
Maximum Waveform Length	2 channels active	32 kSamples	64 kSamples	16 kSamples
Maximum Waveform Length	4 or more channels active	16 kSamples	32 kSamples	8 kSamples
Minimum Number of Averages		2	2	4
Maximum Number of Averages		16777216 (16M)	256	16777216 (16M)
Data Output Format	fixed	32 bit signed integer	16 bit signed integer	32 bit signed integer
Re-Arming Time between waveforms	1.25 GS/s or below	80 samples (+ progra	mmed pretrigger)	80 samples (+ programmed pretrigger)
Re-Arming Time between waveforms	2.5 GS/s	160 samples (+ progr	ammed pretrigger)	160 samples (+ programmed pretrigger)
Re-Arming Time between waveforms	5 GS/s	320 samples (+ progr	ammed pretrigger)	320 samples (+ programmed pretrigger)
Re-Arming Time between end of average to start of next average	0		mmed segment length,	80/160&320 samples as above listed

Block Statistics Signal Processing Option M4i.22xx/DN2.22x Series/DN6.22x Series

Minimum Waveform Length 64 samples Minimum Waveform Stepsize 32 samples

Maximum Waveform Length Standard Acquisition 2 GSamples / channels

Maximum Waveform Length FIFO Acquisition 2 GSamples

Data Output Format fixed 32 bytes statistics summary

Statistics Information Set per Waveform Average, Minimum, Maximum, Position Minimum, Position Maximum, Trigger Timestamp

1.25 GS/s or below Re-Arming Time between Segments 80 samples (+ programmed pretrigger) Re-Arming Time between Segments 2.5 GS/s 160 samples (+ programmed pretrigger) Re-Arming Time between Segments 5 GS/s 320 samples (+ programmed pretrigger)

Multi Purpose I/O lines (front-plate)

Number of multi purpose lines three, named X0, X1, X2

Input: available signal types Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock software programmable

Input: impedance $10~\text{k}\Omega$ to 3.3~VInput: maximum voltage level -0.5 V to +4.0 V 3.3 V LVTTL Input: signal levels

Output: available signal types Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Refclock, System Clock software programmable

Output: impedance Output: signal levels 3.3 V LVTTL

3.3V LVTTL, TTL compatible for high impedance loads Output: type

Output: drive strength Capable of driving 50 Ω loads, maximum drive strength ± 48 mA sampling clock Output: update rate 14bit. 16 bit ADC resolution

Output: update rate 8 bit ADC resolution

Current sampling clock ≤ 1.25 GS/s : sampling clock Current sampling clock > 1.25 GS/s and ≤ 2.50 GS/s : 1/2 sampling clock Current sampling clock > 2.50 GS/s and ≤ 5.00 GS/s : 1/2 sampling clock

Dynamic Parameters

		M4i.223x, M4x.223x and DN2.223-xx, DN2.225-xx and DN6.225-xx, 8 Bit 5 GS/s											
Input Path		DC or AC coupled, fixed 50 Ohm											
Test signal frequency		10 ۸	۸Hz		40 N	۸Hz	70 N	۱Hz	240 N	ΛHz	600 MHz		
Input Range	±200 mV	±500 mV	±1γ	±2.5 V	±200 mV	±1V							
THD (typ) (dB	<-60.2 dB	<-60.3 dB	-<60.3 dB	<-60.3 dB	<-58.9 dB	<-58.2 dB	<-58.8 dB	<-58.0 dB	<-54.0 dB	<-54.0 dB	<-45.0 dB	<-46.3 dB	
SNR (typ) (dB)	>44.5 dB	>44.8 dB	>44.8 dB	>44.5 dB	>44.7 dB	>44.7 dB	>44.3 dB	>44.3 dB	>42.9 dB	>42.9 dB	>40.3 dB	>40.2 dB	
SFDR (typ), excl. harm. (dB)	>53.7 dB	>54.9 dB	>54-9 dB	>54.2 dB	>50.3 dB	>50.8 dB	>50.2 dB	>49.7 dB	>49.4 dB	>49.5 dB	>44.3 dB	>44.6 dB	
SFDR (typ), incl. harm. (dB)	>53.7 dB	>54.7 dB	>54.8 dB	>54.2 dB	>50.3 dB	>50.8 dB	>50.2 dB	>49.7 dB	>49.4 dB	>49.5 dB	>44.3 dB	>44.6 dB	
SINAD/THD+N (typ) (dB)	>44.4 dB	>44.7 dB	>44.7 dB	>44.4 dB	>44.5 dB	>44.4 dB	>44.2 dB	>44.1 dB	>42.6 dB	>42.6 dB	>39.1 dB	>39.3 dB	
ENOB based on SINAD (bit)	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.0 bit	>6.8 bit	>6.8 bit	>6.2 bit	>6.2 bit	
ENOB based on SNR (bit)	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>6.9 bit	>6.9 bit	>6.4 bit	>6.4 bit	

		M4i.222x, M4x.222x and DN2.222-xx, 8 Bit 2.5 G5/s											
Input Path		DC or AC coupled, fixed 50 Ohm											
Test signal frequency		10 A	ΛHz		40 N	ΛHz	70 N	۸Hz	240 MHz		600 MHz		
Input Range	±200 mV	±500 mV	±1 V	±2.5 V	±200 mV	±1V							
THD (typ) (dB	>-56.2 dB	<-56.3 dB	<-56.5 dB	<-56.4 dB	<-55.9 dB	<-55.9 dB	<-54.9 dB	<-55.3 dB	<-53.9 dB	<-53.4 dB	<-43.9 dB	<-45.2 dB	
SNR (typ) (dB)	>45.6 dB	>45.8 dB	>45.6 dB	>45.5 dB	>44.7 dB	>44.9 dB	>44.5 dB	>44.6 dB	>43.9 dB	>44.0 dB	>42.1 dB	>41.9 dB	
SFDR (typ), excl. harm. (dB)	>57.2 dB	>57.3 dB	>55.7 dB	>55.1 dB	>50.9 dB	>50.5 dB	>50.9 dB	>50.6 dB	>49.8 dB	>49.0 dB	>46.3 dB	>45.2 dB	
SFDR (typ), incl. harm. (dB)	>56.5 dB	>56.3 dB	>55.1 dB	>54.5 dB	>50.9 dB	>50.5 dB	>50.9 dB	>50.6 dB	>49.8 dB	>49.0 dB	>45.2 dB	>45.2 dB	
SINAD/THD+N (typ) (dB)	>45.2 dB	>45.4 dB	>45.3 dB	>45.2 dB	>44.4 dB	>44.4 dB	>44.2 dB	>44.3 dB	>43.5 dB	>43.5 dB	>39.9 dB	>40.2 dB	
ENOB based on SINAD (bit)	>7.2 bit	>7.3 bit	>7.2 bit	>7.2 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>6.9 bit	>6.9 bit	>6.3 bit	>6.4 bit	
ENOB based on SNR (bit)	>7.3 bit	>7.3 bit	>7.3 bit	>7.3 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.1 bit	>7.0 bit	>7.0 bit	>6.7 bit	>6.7 bit	

	M4i.	M4i.221x, M4x.221x, DN2.221 and DN6.221-xx, 8 Bit 1.25 GS/s - standard input ranges											
Input Path		DC or AC coupled, fixed 50 Ohm											
Test signal frequency		10 A	ΛHz		40 N	۸Hz	70 MHz		240 MHz				
Input Range	±200 mV	±500 mV	±1γ	±2.5 V	±200 mV	±1V	±200 mV	±1V	±200 mV	±1V			
THD (typ) (dB	<-59.0 dB	<.58.9 dB	<58.9 dB	<59.0 dB	<-53.6 dB	<53.2 dB	<-54.4 dB	<-54.6 dB	<-52.1 dB	<-52.4 dB			
SNR (typ) (dB)	>46.9 dB	>47.0 dB	>47.0 dB	>47.0 dB	>46.8 dB	>47.0 dB	>47.0 dB	>47.0 dB	>46.1 dB	>46.2 dB			
SFDR (typ), excl. harm. (dB)	>62.1 dB	>62.1 dB	>62.2 dB	>62.0 dB	>58.2 dB	>59.8 dB	>62.2 dB	>61.9 dB	>59.5 dB	>58.5 dB			
SFDR (typ), incl. harm. (dB)	>60.7 dB	>60.4 dB	>60.5 dB	>60.4 dB	> 56.1 dB	>56.2 dB	> 57.7 dB	>57.6 dB	>52.5 dB	>52.7 dB			
SINAD/THD+N (typ) (dB)	>46.6 dB	>46.7 dB	>46.7 dB	>46.7 dB	>46.0 dB	>46.1 dB	>46.3 dB	>46.3 dB	>45.1 dB	>45.3 dB			
ENOB based on SINAD (bit)	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.4 bit	>7.4 bit	>7.4 bit	>7.4 bit	>7.2 bit	>7.2 bit			
ENOB based on SNR (bit)	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.5 bit	>7.3 bit	>7.4 bit			

	1	M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s - low voltage input ranges											
Input Path		DC or AC coupled, fixed 50 Ohm											
Test signal frequency		10 /	МНz		40	MHz	70 MHz		240 MHz				
Input Range	±40 mV	±100 mV	±200 mV	±500 vV	±40 mV	±100 mV	±40 mV	±100 mV	±40 mV	±100 mV			
THD (typ) (dB	<-57.0 dB	<.57.0 dB	<.57.1 dB	<.57.2 dB									
SNR (typ) (dB)	>44.0 dB	>44.9 dB	>44.9 dB	>44.9 dB									
SFDR (typ), excl. harm. (dB)	>62.1 dB	>62.1 dB	>62.1 dB	>62.2 dB									
SFDR (typ), incl. harm. (dB)	>60.1 dB	>60.2 dB	>60.2 dB	>60.4 dB									
SINAD/THD+N (typ) (dB)	>44.0 dB	>44.8 dB	>44.8 dB	>44.8 dB									
ENOB based on SINAD (bit)	>7.0 bit	>7.2 bit	>7.2 bit	>7.2 bit									
ENOB based on SNR (bit)	>7.0 bit	>7.2 bit	>7.2 bit	>7.2 bit									

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

RMS Noise Level (Zero Noise)

		M4i.223x, M4x.223x and DN2.223-xx, DN2.225-xx, DN6.225-xx, 8 Bit 5 G\$/s									
Input Range	3	:200 mV	±	500 mV		±1		±2.5 V			
Voltage resolution (1 LSB)	1.6 mV		3.9 mV		7.8 mV		19.5 mV				
DC, fixed 50 Ω , typical	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV			
DC, fixed 50 Ω , maximum	<0.6 LSB	<0.9 mV	<0.6 LSB	<2.3 mV	<0.5 LSB	<4.7 mV	<0.5 LSB	<11.7 mV			

		M4i.222x, M4x.222x and DN2.222-xx, 8 Bit 2.5 GS/s										
Input Range	4	:200 mV	±	500 mV	1	±1	1	±2.5 V				
Voltage resolution (1 LSB)		1.6 mV		3.9 mV		7.8 mV		19.5 mV				
DC, fixed 50 Ω , typical	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV				
DC. fixed 50 Ω . maximum	<0.6 LSB	<0.9 mV	<0.7 LSB	<2.7 mV	<0.5 LSB	<4.7 mV	<0.5 LSB	<11.7 mV				

Standard Version	M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s										
Input Range	±	±200 mV ±500 mV ±1									
Voltage resolution (1 LSB)		1.6 mV		3.9 mV		7.8 mV		19.5 mV			
DC, fixed 50 Ω , typical	<0.2 LSB	<0.3 mV	<0.2 LSB	<0.8 mV	<0.2 LSB	<1.6 mV	<0.2 LSB	<3.9 mV			
DC, fixed 50 Ω , maximum	<0.3 LSB	<0.5 mV	<0.3 LSB	<1.2 mV	<0.3 LSB	<2.3 mV	<0.3 LSB	<5.9 mV			

Low Voltage Version	M4i.221x, M4x.221x and DN2.221-xx, 8 Bit 1.25 GS/s									
Input Range		±40 mV	±100 mV		±200 mV		±	500 mV		
Voltage resolution (1 LSB)		0.3 mV	0.8 mV		1.6 mV		3.9 mV			
DC, fixed 50 Ω, typical	<0.4 LSB	<0.2 mV	<0.4 LSB	<0.3 mV	<0.4 LSB	<0.6 mV	<0.4 LSB	<1.6 mV		
DC, fixed 50 Ω , maximum	<0.5 LSB	<0.2 mV	<0.5 LSB	<0.4 mV	<0.5 LSB	<0.8 mV	<0.5 LSB	<2.0 mV		

Connectors

Analog Inputs/Analog Outputs SMA female (one for each single-ended input) Cable-Type: Cab-3mA-xx-xx Trigger 0 Input SMA female Cable-Type: Cab-3mA-xx-xx Clock Input SMA female Cable-Type: Cab-3mA-xx-xx MMCX female Cable-Type: Cab-1 m-xx-xx Trigger 1 Input Clock Output MMCX female Cable-Type: Cab-1 m-xx-xx Multi Purpose I/O MMCX female (3 lines) Cable-Type: Cab-1 m-xx-xx

Environmental and Physical Details

Dimension (Single Card)

241 mm (¾ PCle length) x 107 mm x 20 mm (single slot width)

Dimension (Card with option SH8tm installed)

241 mm (¾ PCle length) x 107 mm x 40 mm (double slot width)

Dimension (Card with option SH8ex installed)

312 mm (full PCle length) x 107 mm x 20 mm (single slot width)

Weight (M4i.44xx series) maximum 290 g
Weight (M4i.22xx, M4i.66xx, M4i.77xx series) maximum 420 g
Weight (Option star-hub-sh8ex, -sh8tm) including 8 sync cables 130 g
Warm up time 10 minutes

 Warm up time
 10 minutes

 Operating temperature
 0°C to 50°C

 Storage temperature
 -10°C to 70°C

 Humidity
 10% to 90%

PCI Express specific details

PCIe slot type x8 Generation 2
PCIe slot compatibility (physical) x8/x16

PCle slot compatibility (electrical) x1, x4, x8, x16, Generation 1, Generation 2, Generation 3

Sustained streaming mode > 3.4 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PCle x8 Gen2)

Certification, Compliance, Warranty

EMC Immunity Compliant with CE Mark
EMC Emission Compliant with CE Mark

Product warranty 5 years starting with the day of delivery

Software and firmware updates Life-time, free of charge

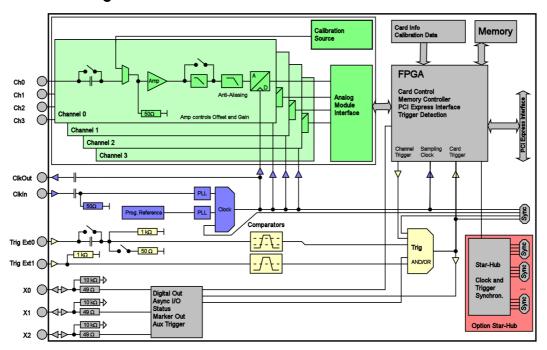
Power Consumption

PCI EXPRESS 3.3V 12 V Total M4i,2230×8, M4i,2220×8, M4i,2210×8 0.2 A 2.6 A 32 W M4i,2233×8, M4i,2221×8, M4i,2211×8 0.2 A 2.7 A 33 W M4i,2233×8, M4i,2211×8 0.2 A 2.9 A 35 W

MTBF

MTBF 100000 hours

Hardware block diagram



Order Information

The card is delivered with 4 GSample on-board memory and supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, ABA mode and Timestamps. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), LabWindows/CVI, IVI, .NET, Delphi, Visual Basic, Java, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASYLab may be available on request.

Adapter cables are not included. Please order separately!

PCI Express x8	Order no.	Bandwid	h Standard mer	m 1 channel	2 channels	4 channels	
_	M4i.2210-x8	500 MH:	z 4 GSample	1.25 GS/s			
	M4i.2211-x8	500 MH:	z 4 GSample	1.25 GS/s	1.25 GS/s		
	M4i.2212-x8	500 MH:	z 4 GSample	1.25 GS/s	1.25 GS/s	1.25 GS/s	
	M4i.2220-x8	1.5 GHz	4 GSample	2.5 GS/s			
	M4i.2223-x8	1.5 GHz	4 GSample	2.5 GS/s	1.25 GS/s		
	M4i.2221-x8	1.5 GHz	4 GSample	2.5 GS/s	2.5 GS/s		
	M4i.2230-x8	1.5 GHz	4 GSample	5 GS/s			
	M4i.2233-x8	1.5 GHz	4 GSample	5 GS/s	2.5 GS/s		
	M4i.2234-x8	1.5 GHz	4 GSample	5 GS/s	2.5 GS/s	1.25 GS/s	
Options	Order no.	Option					
	M4i.22xx-ir40m		ge input range optio ', bandwidth limited t		Input ranges with ±	40 mV, ±100 mV, ±20	00 mV,
<u>Options</u>	Order no.	Option					
	M4i.xxxx-SH8ex (1)		ization Star-Hub for u xpress length (312 m			vidth, extension of the	card to
	M4i.xxxx-SH8tm (1)		ization Star-Hub for a ion cables included.	up to 8 cards (top mo	ount), two slots wid	h, top mounted on car	rd. 8 syn-
	M4i-upgrade	Upgrade	for M4i.xxxx: Later i	nstallation of option	Star-Hub		
Firmware Options	Order no.	Option			4 . 6		
	M4i.xxxx-spavg M4i.xxxx-spstat	_	ocessing Firmware C ocessing Firmware C			pgrade available) · firmware - upgrade a	vailable)
Services	Order no.						
	Recal	Recalibra	tion at Spectrum incl	. calibration protoco			
Standard Cables			Order no.				
Sidiladia Cabics	for Connections	Length	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
	Analog/Clock-In/Trig-In	80 cm	Cab-3mA-9m-80	Cab-3mA-9f-80	10 ON THICK	io orth (lemaic	10 GIVIS TETRAIC
	Analog/Clock-In/Trig-In	200 cm	Cab-3mA-9m-200	Cab-3mA-9f-200			
	Probes (short)	5 cm		Cab-3mA-9f-5			
	Clk-Out/Trig-Out/Extra	80 cm	Cab-1 m-9 m-80	Cab-1 m-9f-80	Cab-1m-3mA-80	Cab-1 m-3fA-80	Cab-1 m-3f-80
	Clk-Out/Trig-Out/Extra	200 cm	Cab-1 m-9 m-200	Cab-1 m-9f200	Cab-1 m-3 mA-200	Cab-1 m-3fA-200	Cab-1 m-3f-200
	Information					nominal attenuation of which was cables series Cl	of 0.3 dB/m at 100 MHz and HF
Low Loss Cables	Order No.	Option					
	CHF-3mA-3mA-200	Low loss	cables SMA male to	SMA male 200 cm			
	CHF-3mA-9m-200	Low loss	cables SMA male to	BNC male 200 cm			
	Information					n attenuation of 0.3 dl of 200 MHz and abo	B/m at 500 MHz and ove.
<u>Amplifiers</u>	Order no.	Bandwid	h Connection	Input Impedo	ance Coupling	Amplification	
	SPA.1841 (2)	2 GHz	SMA	50 Ohm	AC	×100 (40 dB)	
	SPA.1801 (2)	2 GHz	SMA	50 Ohm	AC	×10 (20 dB)	
	SPA.1601 (2)	500 MH:	z BNC	50 Ohm	DC	×10 (20 dB)	
	Information	ually swit	chable settings. An e	external power supply	for 100 to 240 V		nanually adjustable offset, man- be sure to order an adapter card input
		Subject ind	go ap.iiioi c				
<u>Software SBench6</u>	Order no.						
	SBench6		ion included in deliv				
	SBenchó-Pro		nal version for one co		•		
	SBench6-Multi		•		es multiple synchro	nized cards in one sys	tem.
	Volume Licenses	Please as	k Spectrum for detail	S.			
Software Options	Order no.						
	SPc-RServer SPc-SCAPP	Spectrum	's CUDA Access for F	Parallel Processing - S	DK for direct data	M4i/M4x/M2p cards ransfer between Spect	trum card
		and CUD	A GPU. Includes RDI	MA activation and ex	camples. Signed N	DA needed for access.	

^{(1):} Just one of the options can be installed on a card at a time

Technical changes and printing errors possible

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