DN2.82x - hybridNETBOX up to 500 MS/s Digitizer and 1.25 GS/s AWG

- Stimulus-Response, Closed-Loop, Recorder/Replay, Automated Tests, MIMO, ...
- 2 or 4 channels Digitizer with 180 MS/s up to 500 MS/s
- 2 or 4 channels AWG with 625 MS/s up to 1.25 GS/s
- Simultaneously sampling and generation on all channels
- 2 GSample acquisition and 2 GSample AWG memory
- Digitizer: separate ADC and amplifier per channel
- Digitizer: 6 input ranges: ±200 mV up to ±10 V
- Digitizer: programmable input offset of ±100%
- AWG: output into 50 Ohm up to ±2.5 V (4 channels) or ±2 V (2 channels)
- AWG: output into 1 MOhm up to ±5 V (4 channels) or ±4 V (2 channels)
- Streaming, Multiple Recording, Gated Sampling, Timestamps, Sequence Replay

SBench 6 can only operate the cards independently by starting two instances of the program:

- Stimulus-Response, Closed-Loop, Recorder/Replay, Automated Tests, MIMO, ...
- 2 or 4 channels Digitizer with 180 MS/s up to 500 MS/s
- 2 or 4 channels AWG with 625 MS/s up to 1.25 GS/s
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- Streaming, Multiple Recording, Gated Sampling, Timestamps, Sequence Replay

**Operating Systems**
- Windows 7 (SP1), 8, 10, Server 2008 R2 and newer
- Linux Kernel 2.6, 3.x, 4.x, 5.x
- Windows/Linux 32 and 64 bit

**SBench 6 Professional Included**
- Acquisition, Generation and Display of analog and digital data
- Calculation, FFT
- Documentation and Import, Export

**Drivers**
- LabVIEW, MATLAB, LabWindows/CVI
- Visual C++, C++ Builder, GNU C++, VB.NET, C#, J#, Delphi, Java, Python
- NI

**Export-Versions**
Sampling rate limited versions that do not fall under export restrictions.

<table>
<thead>
<tr>
<th>Model</th>
<th>Channels</th>
<th>Digitizer Res.</th>
<th>Sampling Rate</th>
<th>Arbitrary Waveform Generator Channels</th>
<th>Res.</th>
<th>Sampling Rate</th>
<th>Output Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>DN2.822-02</td>
<td>2 channels</td>
<td>16 bit</td>
<td>250 MS/s</td>
<td>2 channels</td>
<td>16 bit</td>
<td>1.25 GS/s</td>
<td>±2.0 V (50Ω)</td>
</tr>
<tr>
<td>DN2.822-04</td>
<td>4 channels</td>
<td>16 bit</td>
<td>250 MS/s</td>
<td>4 channels</td>
<td>16 bit</td>
<td>625 MS/s</td>
<td>±2.5 V (50Ω)</td>
</tr>
<tr>
<td>DN2.825-02</td>
<td>2 channels</td>
<td>14 bit</td>
<td>500 MS/s</td>
<td>2 channels</td>
<td>16 bit</td>
<td>1.25 GS/s</td>
<td>±2.0 V (50Ω)</td>
</tr>
<tr>
<td>DN2.825-04</td>
<td>4 channels</td>
<td>14 bit</td>
<td>500 MS/s</td>
<td>4 channels</td>
<td>16 bit</td>
<td>625 MS/s</td>
<td>±2.5 V (50Ω)</td>
</tr>
<tr>
<td>DN2.827-02</td>
<td>2 channels</td>
<td>16 bit</td>
<td>180 MS/s</td>
<td>2 channels</td>
<td>16 bit</td>
<td>1.25 GS/s</td>
<td>±2.0 V (50Ω)</td>
</tr>
<tr>
<td>DN2.827-04</td>
<td>4 channels</td>
<td>16 bit</td>
<td>180 MS/s</td>
<td>4 channels</td>
<td>16 bit</td>
<td>625 MS/s</td>
<td>±2.5 V (50Ω)</td>
</tr>
<tr>
<td>DN2.828-02</td>
<td>2 channels</td>
<td>14 bit</td>
<td>400 MS/s</td>
<td>2 channels</td>
<td>16 bit</td>
<td>1.25 GS/s</td>
<td>±2.0 V (50Ω)</td>
</tr>
<tr>
<td>DN2.828-04</td>
<td>4 channels</td>
<td>14 bit</td>
<td>400 MS/s</td>
<td>4 channels</td>
<td>16 bit</td>
<td>625 MS/s</td>
<td>±2.5 V (50Ω)</td>
</tr>
</tbody>
</table>

**General Information**
The hybridNETBOX DN2.82x series internally consists of a Digitizer and an AWG that can run together or independently. That allows simultaneous data generation and data acquisition for stimulus-response tests, ATE applications, MIMO applications or closed-loop applications. The hybridNETBOX can be installed anywhere in the company LAN and can be remotely controlled from a host PC.

Synchronization is done externally with the help of clock/trigger-output to clock/trigger-input connection.
Software Support

Windows Support
The digitizerNETBOX/generatorNETBOX/hybridNETBOX can be accessed from Windows 7, Windows 8, Windows 10 (each 32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, LabWindows/CVI, Delphi, Visual Basic, VB.NET, C#, J#, Python, Java and IVI are included.

Linux Support
The digitizerNETBOX/generatorNETBOX/hybridNETBOX can be accessed from any Linux system. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++, Python as well as drivers for MATLAB for Linux. SBench 6, the powerful data acquisition and analysis software from Spectrum is also included as a Linux version.

Discovery Protocol
The Discovery function helps you to find and identify any Spectrum LXI instruments, like the digitizerNETBOX and generatorNETBOX, available to your computer on the network. The Discovery function will also locate any Spectrum card products that are managed by an installed Spectrum Remote Server somewhere on the network.

After running the discovery function the card information is cached and can be directly accessed by SBench 6. Furthermore the qualified VISA address is returned and can be used by any software to access the remote instrument.

SBench 6 Professional
The digitizerNETBOX, generatorNETBOX and hybridNETBOX can be used with Spectrum’s powerful software SBench 6 – a Professional license for the software is already installed in the box. SBench 6 supports all of the standard features of the instrument. It has a variety of display windows as well as analysis, export and documentation functions.

- Available for Windows Windows 7, Windows 8, Windows 10 and Linux
- Easy to use interface with drag and drop, docking windows and context menus
- Display of analog and digital data, X-Y display, frequency domain and spread signals
- Designed to handle several GBytes of data
- Fast data preview functions
- SBench 6 only supports either AWG or Digitizer in one program
- StarHub for mixed mode applications is not supported
- To run AWG and Digitizer with SBench 6, the software needs to be started twice and each instance of the program then operates independently one device

Third-party Software Products
Most popular third-party software products, such as LabVIEW, MATLAB or LabWindows/CVI are supported. All drivers come with examples and detailed documentation.

IVI Driver
The IVI standards define an open driver architecture, a set of instrument classes, and shared software components. Together these provide critical elements needed for instrument interchangeability. IVI’s defined Application Programming Interfaces (APIs) standardize common measurement functions reducing the time needed to learn a new IVI instrument.

The Spectrum products to be accessed with the IVI driver can be locally installed data acquisition cards, remotely installed data acquisition cards or remote LXI instruments like digitizerNETBOX/generatorNETBOX. To maximize the compatibility with existing IVI based software installations, the Spectrum IVI driver supports IVI Scope, IVI Digitizer and IVI FGen class with IVC and IVI-COM interfaces.
General Hardware features and options

LXI Instrument

The digitizerNETBOX and generatorNETBOX are fully LXI instrument compatible to LXI Core 2011 following the LXI Device Specification 2011 rev. 1.4. The digitizerNETBOX/generatorNETBOX has been tested and approved by the LXI Consortium. Located on the front panel is the main on/off switch, LEDs showing the LXI and Acquisition status and the LAN reset switch.

Chassis features

- stable metal chassis
- 8 bumper edges protect the chassis, the desk and other components on it. The bumper edges allow to store the chassis either vertically or horizontally and the lock-in structure allows to stack multiple chassis with a secure fit onto each other. For 19" rack mount montage the bumpers can be unmounted and replaced by the 19" rack mount option
- The handle allows to easily carry the chassis around in just one hand.
- A standard GND screw on the back of the chassis allows to connect the metal chassis to measurement ground to reduce noise based on ground loops and ground level differences.

Front Panel

Standard BNC connectors are used for all analog input or output signals and all auxiliary signals like clock and trigger. No special adapter cables are needed and the connection is secure even when used in a moving environment.

Custom front panels are available on request even for small series, be it SMA, LEMO connectors or custom specific connectors.

Ethernet Connectivity

The GBit Ethernet connection can be used with standard COTS Ethernet cabling. The integration into a standard LAN allows to connect the digitizerNETBOX/generatorNETBOX either directly to a desktop PC or Laptop or it is possible to place the instrument somewhere in the company LAN and access it from any desktop over the LAN.

Boot on Power Option

The digitizerNETBOX/generatorNETBOX can be factory configured to automatically start and boot upon availability of the input power rail. That way the instrument will automatically become available again upon loss of input power.

DC Power Supply Option

The digitizerNETBOX/generatorNETBOX can be equipped with an internal DC power supply which replaces the standard AC power supply. Two different power supply options are available that range from 9V to 36V. Contact the sales team if other DC levels are required.

Using the DC power supply the digitizerNETBOX/generatorNETBOX can be used for mobile applications together with a Laptop in automotive or airborne applications.

Option Embedded Server

The option turns the digitizerNETBOX/generatorNETBOX in a powerful PC that allows to run own programs on a small external clock

Using a dedicated connector a sampling clock can be fed in from an external reference clock (normally 10 MHz) is necessary to synchronize external equipment to this clock.

Reference clock

The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Export Versions

Special export versions of the products are available that do not fall under export control. Products fall under export control if their specification exceeds certain sampling rates at a given A/D resolution and if the product is shipped into a country where no general export authorization is in place.

The export versions of the products have a sampling rate limitation matching the export control list. An upgrade to the faster version is not possible. The sampling rate limitation is in place for both internal and external clock.
**Digitizer Hardware Features and Options**

**Input Amplifier**

The analog inputs can be adapted to real-world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 Mohm, one can select a matching input range and the signal offset can be compensated by programmable AC coupling. The latest hardware revisions additionally allow for offset compensation for DC-coupled inputs as well.

**Software selectable input path**

For each of the analog channels the user has the choice between two analog input paths. The “Buffered” path offers the highest flexibility when it comes to input ranges and termination. A software programmable 50 Ohm and 1 Mohm termination also allows to connect standard oscilloscope probes to the card. The “50 Ohm” path on the other hand provides the highest bandwidth and the best signal integrity with a fewer number of input ranges and a fixed 50 Ohm termination.

**Software selectable lowpass filter**

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be useful especially with low voltage input signals.

**Automatic on-board calibration**

All of the channels are calibrated in factory before the board is shipped. To compensate for different variations like PC power supply, temperature and aging, the software driver provides routines for an automatic onboard offset and gain calibration of all input ranges. All the cards contain a high precision on-board calibration reference.

**Ring buffer mode**

The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

**FIFO mode**

The FIFO mode is designed for continuous data transfer between remote instrument and PC memory or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

**Channel trigger**

The data acquisition instruments offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it’s also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

**External trigger input**

All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

**Multiple Recording**

The Multiple Recording mode allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn’t need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

**Gated Sampling**

The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

**Timestamp**

The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

**ABA mode**

The ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

**Boxcar Average (high-resolution) mode**

The Boxcar average or high-resolution mode is a form of averaging. The ADC oversamples the signal and averages neighboring points together. This mode uses a real-time boxcar averaging algorithm that helps reducing random noise. It also can yield a higher number of bits of resolution depending on the signal acquired. The averaging factor can be set in the region of 2 to 256. Averaged samples are stored as 32 bit values and can be processed by any software. The trigger detection is still running with
full sampling speed allowing a very precise relation between acquired signal and the trigger.

**Firmware Option Block Average**

The Block Average Module improves the fidelity of noisy repetitive signals. Multiple repetitive acquisitions with very small dead-time are accumulated and averaged. Random noise is reduced by the averaging process improving the visibility of the repetitive signal. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

**Firmware Option Block Statistics (Peak Detect)**

The Block Statistics and Peak Detect Module implements a widely used data analysis and reduction technology in hardware. Each block is scanned for minimum and maximum peak and a summary including minimum, maximum, average, timestamps and position information is stored in memory. The complete averaging process is done inside the FPGA of the digitizer generating no CPU load at all. The amount of data is greatly decreased as well as the needed transfer bandwidth is heavily reduced.

Please see separate data sheet for details on the firmware option.

**AWG Hardware Features and Options**

**Singleshot output**

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

**Repeated output**

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

**Single Restart replay**

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

**FIFO mode**

The FIFO mode is designed for continuous data transfer between PC memory or hard disk and the generation board. The control of the data stream is done automatically by the driver on an interrupt request basis. The complete installed on-board memory is used for buffering data, making the continuous streaming extremely reliable.

**Multiple Replay**

The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

**Gated Replay**

The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a programmed level.

**Sequence Mode**

The sequence mode allows to split the card memory into several data segments of different length. These data segments are chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed. All trigger-related and software-command-related functions are only working on single cards, not on star-hub-synchronized cards.

**External trigger input**

All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.
hybridNETBOX Technical Data - Digitizer

### Analog Inputs

<table>
<thead>
<tr>
<th>Resolution</th>
<th>130 MS/s up to 250 MS/s</th>
<th>400 MS/s and 500 MS/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Type</td>
<td>Single-ended</td>
<td></td>
</tr>
<tr>
<td>ADC Differential non linearity (DNL)</td>
<td>±0.5 LSB (14 Bit ADC), ±0.4 LSB (16 Bit ADC)</td>
<td></td>
</tr>
<tr>
<td>ADC Integral non linearity (INL)</td>
<td>±2.5 LSB (14 Bit ADC), ±10.0 LSB (16 Bit ADC)</td>
<td></td>
</tr>
<tr>
<td>ADC Word Error Rate (WER)</td>
<td>max. sampling rate 10/2</td>
<td></td>
</tr>
<tr>
<td>Channel selection</td>
<td>software programmable</td>
<td>1, 2, or 4 (maximum is model dependent)</td>
</tr>
<tr>
<td>Bandwidth filter</td>
<td>activate by software</td>
<td>20 MHz bandwidth with 3rd order Butterworth filtering</td>
</tr>
</tbody>
</table>

#### Trigger

<table>
<thead>
<tr>
<th>Trigger level resolution</th>
<th>software programmable</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Crossovers 1 MHz sine signal</th>
<th>range ±1V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crossovers 20 MHz sine signal</td>
<td>range ±1V</td>
</tr>
<tr>
<td>Crossovers 1 MHz sine signal</td>
<td>range ±5V</td>
</tr>
<tr>
<td>Crossovers 20 MHz sine signal</td>
<td>range ±5V</td>
</tr>
</tbody>
</table>

### Multi Purpose I/O lines (front-plate)

<table>
<thead>
<tr>
<th>Number of multi purpose lines</th>
<th>three, named X0, X1, X2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input available signal types</td>
<td>Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock</td>
</tr>
<tr>
<td>Input: impedance</td>
<td>10 kΩ to 3.3 V</td>
</tr>
<tr>
<td>Input: maximum voltage level</td>
<td>0.5 V to +4.0 V</td>
</tr>
<tr>
<td>Input: signal levels</td>
<td>3.3 V LVTTL</td>
</tr>
<tr>
<td>Input: bandwidth</td>
<td>125 MHz</td>
</tr>
<tr>
<td>Output available signal types</td>
<td>Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Reference, System Clock</td>
</tr>
<tr>
<td>Output: impedance</td>
<td>50.0 V</td>
</tr>
<tr>
<td>Output: signal levels</td>
<td>3.3 V LVTTL</td>
</tr>
<tr>
<td>Output: type</td>
<td>3.3V LVTTL, TTL compatible for high impedance loads</td>
</tr>
<tr>
<td>Output: drive strength</td>
<td>Capable of driving 50 Ω loads, maximum drive strength ±48 mA</td>
</tr>
</tbody>
</table>

#### ADC Resolution

<table>
<thead>
<tr>
<th>ADC Resolution</th>
<th>16 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>max sampling clock</td>
<td>1.30 MS/s</td>
</tr>
<tr>
<td>min sampling clock (standard clock mode)</td>
<td>3.814 kS/s</td>
</tr>
<tr>
<td>min sampling clock (special clock mode)</td>
<td>0.610 kS/s</td>
</tr>
</tbody>
</table>

#### Buffered (high impedance) Path

<table>
<thead>
<tr>
<th>Buffered (high impedance) Path</th>
<th>50 Ω (HF) Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Path Types</td>
<td>software programmable</td>
</tr>
<tr>
<td>Programmable Input Offset</td>
<td>not available</td>
</tr>
<tr>
<td>Programmable Input Offset (Frontend HW/Version &lt; V9)</td>
<td>±100.0% on all ranges</td>
</tr>
<tr>
<td>Offset error (full speed)</td>
<td>&lt; 0.1% of range</td>
</tr>
<tr>
<td>Over voltage protection</td>
<td>±2 V rms</td>
</tr>
<tr>
<td>Max DC voltage if AC coupling active</td>
<td>±30 V</td>
</tr>
</tbody>
</table>

#### Relative input stage delay

| Bandwidth filter disabled: 0 ns |
| Bandwidth filter enabled: 14.7 ns |

| Crosstalk 1 MHz sine signal range ±1V | ≤96 dB |
| Crosstalk 20 MHz sine signal range ±1V | ≤82 dB |
| Crosstalk 1 MHz sine signal range ±5V | ≤97 dB |
| Crosstalk 20 MHz sine signal range ±5V | ≤82 dB |

### Output

| Output: available signal types | Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Reference, System Clock |
| Input available signal types | Asynchronous Digital-In, Synchronous Digital-In, Timestamp Reference Clock |
| Input: maximum voltage level | 0.5 V to +4.0 V |
| Input: signal levels | 3.3 V LVTTL |
| Input: bandwidth | 125 MHz |
| Output available signal types | Asynchronous Digital-Out, Trigger Output, Run, Arm, PLL Reference, System Clock |
| Output: impedance | 50.0 V |
| Output: signal levels | 3.3 V LVTTL |
| Output: type | 3.3V LVTTL, TTL compatible for high impedance loads |
| Output: drive strength | Capable of driving 50 Ω loads, maximum drive strength ±48 mA |
| Output: update rate | 14-bit or 16-bit ADC resolution sampling clock |
| Output: update rate | 7-bit or 8-bit ADC resolution current sampling clock |

| Current sampling clock < 1.25 Gs/s: sampling clock |
| Current sampling clock > 1.25 Gs/s: sampling clock |
| Current sampling clock > 2.50 Gs/s: sampling clock |
| Current sampling clock > 5.00 Gs/s: sampling clock |

<table>
<thead>
<tr>
<th>ADC Resolution</th>
<th>16 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>max sampling clock</td>
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</tr>
<tr>
<td>min sampling clock (special clock mode)</td>
<td>0.610 kS/s</td>
</tr>
</tbody>
</table>
## RMS Noise Level (Zero Noise), typical figures

### Dynamic Parameters

<table>
<thead>
<tr>
<th>M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s</th>
<th>M4i.444x, M4x.444x, DN2.444-xx and DN6.444-xx, 14 Bit 250 MS/s</th>
<th>M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s</th>
<th>M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Range</strong></td>
<td>±200 mV</td>
<td>±500 mV</td>
<td>±1 V</td>
</tr>
<tr>
<td><strong>Voltage resolution</strong></td>
<td>24.4 µV</td>
<td>61.2 µV</td>
<td>122 µV</td>
</tr>
</tbody>
</table>

### Input Path

- **HF path, DC, fixed 50 Ω**
- **Buffered path, full bandwidth**
- **Buffered path, BW limit active**

### Input Range

<table>
<thead>
<tr>
<th>±1.0 LSB</th>
<th>±2.0 LSB</th>
<th>±3.0 LSB</th>
<th>±4.1 LSB</th>
<th>±5.7 LSB</th>
<th>±7.8 LSB</th>
<th>±10.7 LSB</th>
<th>±12.1 LSB</th>
<th>±15.3 LSB</th>
<th>±19.0 LSB</th>
<th>±24.4 LSB</th>
<th>±31.0 LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>±9.1 LSB</td>
<td>±16.3 LSB</td>
<td>±23.8 LSB</td>
<td>±48.8 LSB</td>
<td>±83.6 LSB</td>
<td>±128.0 LSB</td>
<td>±172.8 LSB</td>
<td>±217.2 LSB</td>
<td>±261.9 LSB</td>
<td>±316.2 LSB</td>
<td>±380.8 LSB</td>
<td>±445.0 LSB</td>
</tr>
</tbody>
</table>

### Test signal frequency

<table>
<thead>
<tr>
<th>1 MHz</th>
<th>10 MHz</th>
<th>40 MHz</th>
<th>70 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>±3.5 LSB</td>
<td>±6.1 LSB</td>
<td>±9.7 LSB</td>
<td>±13.3 LSB</td>
</tr>
<tr>
<td>±6.0 LSB</td>
<td>±11.0 LSB</td>
<td>±16.0 LSB</td>
<td>±22.0 LSB</td>
</tr>
</tbody>
</table>

### SNR (typ) (dB)

1. **M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s**
2. **M4i.444x, M4x.444x, DN2.444-xx and DN6.444-xx, 14 Bit 250 MS/s**
3. **M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s**
4. **M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s**

### SFDR (typ), excl. harm. (dB)

1. **M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s**
2. **M4i.444x, M4x.444x, DN2.444-xx and DN6.444-xx, 14 Bit 250 MS/s**
3. **M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s**
4. **M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s**

### ENOB based on SNR (bit)

1. **M4i.445x, M4x.445x, DN2.445-xx and DN6.445-xx, 14 Bit 500 MS/s**
2. **M4i.444x, M4x.444x, DN2.444-xx and DN6.444-xx, 14 Bit 250 MS/s**
3. **M4i.442x, M4x.442x, DN2.442-xx and DN6.442-xx, 16 Bit 250 MS/s**
4. **M4i.447x, M4x.447x, DN2.447-xx and DN6.447-xx, 16 Bit 180 MS/s**
### Noise Floor Plots (open inputs)

![Noise Floor Plots](image)

#### Connectors

<table>
<thead>
<tr>
<th>Connector</th>
<th>SMA female (one for each single-ended input)</th>
<th>Cable-Type: Cab-3mA-xx-xx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Channels</td>
<td></td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>Clock Input</td>
<td>SMA female</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>Clock Output</td>
<td>SMA female</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>Trg0 Input</td>
<td>SMA female</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>Trg1 Input</td>
<td>SMA female</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>X0/Trigger Output/Timestamp Clock</td>
<td>programmable direction</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>X1</td>
<td>programmable direction</td>
<td>Cab-3mA-xx-xx</td>
</tr>
<tr>
<td>X2</td>
<td>programmable direction</td>
<td>Cab-3mA-xx-xx</td>
</tr>
</tbody>
</table>
hybridNETBOX Technical Data - Arbitrary Waveform Generator

### Analog Outputs

- **Resolution**: 16 bit
- **D/A Interpolation**: no interpolation

| M4i.662x/M4x.662x | M4i.663x/M4x.663x | High bandwidth version
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DN2.662/DN6.662x</td>
<td>DN6.663/DN6.663x</td>
<td>1.25 GS/s + option-hbw</td>
</tr>
</tbody>
</table>

#### Output Amplitude

- **50Ω termination**: ±80 mV up to ±3.5 V
- **High impedance**: ±160 mV up to ±4 V

#### Step sizes

- **50Ω termination**: 1 mV
- **High impedance**: 2 mV

#### Rise/Fall time

- **50Ω termination**: 1.06 µs
- **High impedance**: n.a.

#### Output Offset

- **Fixed**: 0 V

#### Output Amplifier Path Selection

- **Low Power path**: ±80 mV to ±480 mV (into 50Ω)
- **High Power path**: ±420 mV to ±2.5 V/±2 V (into 50Ω)

#### Output Amplifier Setting Hysteresis

- **Automatic**: 420 mV to 480 mV (if output is using low power path it will switch to high power path at 480 mV. If output is using high power path it will switch to low power path at 420 mV)

#### Filters

- **Software programmable**: bypass with no filter or one fixed filter

#### Output Resistance

- **50Ω**

#### Minimum output load

- **0Ω** (short circuit safe)

#### Output Accuracy

- **Low power path**: ±0.5 mV ±0.1% of programmed output amplitude
- **High power path**: ±1.0 mV ±0.2% of programmed output amplitude

### Trigger

- **Available trigger modes**: software programmable
- **External**: Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)

#### Trigger edge

- **Rising edge**, **falling edge** or both edges

#### Trigger delay

- **Software programmable**: 0 to (8GSamples - 32) = 8589934560 Samples in steps of 32 samples

#### Multi, Gate: re-arming time

- **40 samples**

#### Trigger to Output Delay

- **Sample rate ≤ 625 MS/s**: 238.5 sample clocks + 16 ns
- **Sample rate > 625 MS/s**: 476.5 sample clocks + 16 ns

#### Memory depth

- **32 up to [installed memory / number of active channels] samples in steps of 32**

#### Multiple Replay segment size

- **16 up to [installed memory / 2 / active channels] samples in steps of 16**

#### Minimum external trigger pulse width

- **≥ 2 samples**

### External trigger

- **Impedance**: 50Ω / 1 kΩ
- **Coupling**: AC or DC
- **Type**: Window comparator, Single level comparator
- **Input level**: ±10 V (1 kΩ), ±2.5 V (50Ω)
- **Sensitivity**: 2.5% of full scale range
- **Maximum voltage**: ±30 V
- **Bandwidth DC**: 50 Ω
- **AC**: 1 kHz
- **Minimum external trigger pulse width**: ≥ 2 samples

### Multi Purpose I/O lines (front-plate)

- **Number of multi purpose lines**: three, named X0, X1, X2
- **Input available signal types**: Asynchronous Digital-In
- **Input impedance**: 10 kΩ to 3.3 V
- **Input maximum voltage level**: ±0.5 V to ±4.0 V
- **Input signal levels**: 3.3 V (LVTT)
- **Output available signal types**: Asynchronous Digital-Out, Synchronous Digital-Out, Trigger Output, Run, Arm, Marker Output, System Clock
- **Output impedance**: 50 Ω
- **Output signal levels**: 3.3 V (LVTT), TTL compatible for high impedance loads
- **Output drive strength**: Capable of driving 50Ω loads, maximum drive strength ±48 mA
- **Output update rate**: sampling clock
**Sequence Replay Mode (Mode available starting with firmware V1.14)**

- **Number of sequence steps**: software programmable, 1 up to 4096 (sequence steps can be overloaded at runtime)
- **Number of memory segments**: software programmable, 2 up to 64k (segment data can be overloaded at runtime)
- **Minimum segment size**: software programmable, 384 samples (1 active channel), 192 samples (2 active channels), 96 samples (4 active channels), in steps of 32 samples.
- **Maximum segment size**: software programmable, 2 GS / active channels / number of sequence segments (round up to the next power of two)
- **Loop Count**: software programmable, 1 to (1M - 1) loops
- **Sequence Step Commands**: software programmable, Loop for #Loops, Next, Loop until Trigger, End Sequence
- **Special Commands**: software programmable, Data Overload at runtime, sequence steps overload at runtime, readout current replayed sequence step
- **Limitations for synchronized products**: Software commands changing the sequence as well as „Loop until trigger” are not synchronized between cards. This also applies to multiple AWG modules in a generatorNETBOX.

**Clock**

- **Clock Modes**: software programmable, internal PLL, external reference clock, Star-Hub sync (M4i only), PXI Reference Clock (M4x only)
- **Internal clock accuracy**: ≤±20 ppm
- **Internal clock setup granularity**: 8 Hz (internal reference clock only, restrictions apply to external reference clock)
- **Settable Clock speeds**: 50 MHz to max sampling clock
- **Clock Setting Gaps**: 750 to 757 MHz, 1125 to 1145 MHz (no sampling clock possible in these gaps)
- **External reference clock range**: software programmable, ≥10 MHz and ≤1.25 GHz
- **External reference clock input impedance**: 50Ω fixed
- **External reference clock input coupling**: AC coupling
- **External reference clock input edge**: Rising edge
- **External reference clock input type**: Single-ended, sine wave or square wave
- **External reference clock input swing**: square wave 0.3 V peak-peak up to 3.0 V peak-peak
- **External reference clock input swing**: sine wave 1.0 V peak-peak up to 3.0 V peak-peak
- **External reference clock input max DC voltage**: ±30 V (with max 3.0 V difference between low and high level)
- **External reference clock input duty cycle requirement**: 45% to 55%
- **External reference clock output type**: Single-ended, 3.3V LVPECL
- **Clock output**: sampling clock ≤71.68 MHz
- **Clock output**: sampling clock >71.68 MHz
- **Star-Hub synchronization clock modes**: software selectable, Internal clock, external reference clock

<table>
<thead>
<tr>
<th>Filter</th>
<th>3dB bandwidth</th>
<th>Filter characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter 0</td>
<td>70 MHz</td>
<td>third-order Butterworth</td>
</tr>
<tr>
<td>Filter 1</td>
<td>20 MHz</td>
<td>fifth-order Butterworth</td>
</tr>
<tr>
<td>Filter 2</td>
<td>5 MHz</td>
<td>fourth-order Bessel</td>
</tr>
<tr>
<td>Filter 3</td>
<td>1 MHz</td>
<td>fourth-order Bessel</td>
</tr>
</tbody>
</table>

**Bandwidth and Filters**

- **Analog bandwidth does not include Sinc response of DAC**
**Dynamic Parameters**

<table>
<thead>
<tr>
<th>M2p.653x/DNx.653-xx/DNx.803-xx</th>
<th>M2p.654x/DNx.654-xx/DNx.813-xx</th>
<th>M2p.656x/DNx.656-xx/DNx.806-xx</th>
<th>M2p.657x/DNx.657-xx/DNx.816-xx</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test - Samplerate</strong></td>
<td>40 MS/s</td>
<td>40 MS/s</td>
<td>125 MS/s</td>
</tr>
<tr>
<td><strong>Output Frequency</strong></td>
<td>800 kHz</td>
<td>4 MHz</td>
<td>800 kHz</td>
</tr>
<tr>
<td><strong>Output Level in 50 Ω</strong></td>
<td>±900mV</td>
<td>±3000mV</td>
<td>±900mV</td>
</tr>
<tr>
<td><strong>Used Filter</strong></td>
<td>1 MHz</td>
<td>5 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td><strong>NSD (typ)</strong></td>
<td>-142 dBm/Hz</td>
<td>-132 dBm/Hz</td>
<td>-142 dBm/Hz</td>
</tr>
<tr>
<td><strong>SNR (typ)</strong></td>
<td>90.7 dB</td>
<td>91.1 dB</td>
<td>83.7 dB</td>
</tr>
<tr>
<td><strong>THD (typ)</strong></td>
<td>-74.0 dB</td>
<td>-74.0 dB</td>
<td>-70.5 dB</td>
</tr>
<tr>
<td><strong>SINAD (typ)</strong></td>
<td>73.8 dB</td>
<td>73.8 dB</td>
<td>73.6 dB</td>
</tr>
<tr>
<td><strong>SFDR (typ), excl harm.</strong></td>
<td>12.0</td>
<td>12.0</td>
<td>11.3</td>
</tr>
<tr>
<td><strong>ENOB (SINAD)</strong></td>
<td>14.7</td>
<td>14.8</td>
<td>13.5</td>
</tr>
<tr>
<td><strong>ENOB (SNR)</strong></td>
<td>14.1</td>
<td>14.3</td>
<td>13.6</td>
</tr>
</tbody>
</table>

THD and SFDR are measured at the given output level and 50 Ohm termination with a high resolution M3i.4860/M4i.4450-x8 data acquisition card and are calculated from the spectrum. Noise Spectral Density is measured with built-in calculation from an HP E4401B Spectrum Analyzer. All available D/A channels are activated for the tests. SNR and SFDR figures may differ depending on the quality of the used PC. NSD = Noise Spectral Density, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range.
hybridNETBOX Technical Data - General

Option digitizerNETBOX/generatorNETBOX embedded server (DN2.xxx-Emb, DN6.xxx-Emb)

- **CPU**: Intel Quad Core 2 GHz
- **System memory**: 4 GByte RAM
- **System data storage**: Internal 128 GByte SSD
- **Development access**: Remote Linux command shell [ssh], no graphical interface (GUI) available
- **Accessible Hardware**: Full access to Spectrum instruments, LAN, front panel LEDs, RAM, SSD
- **Integrated operating system**: OpenSuse 12.2 with kernel 4.4.7
- **Power connection details**: Mains AC power supply, Input voltage: 100 to 240 VAC, 50 to 60 Hz, AC power supply connector, IEC 60320-1-C14 (PC standard coupler), Power supply cord, power cord included for Schuko contact (CEE 7/7)

Ethernet specific details

- **LAN Connection**: Standard RJ45
- **LAN Speed**: Auto Sensing: GBit Ethernet, 100BASE-T, 10BASE-T
- **LAN IP address**: DHCP [IPv4] with AutoIP fallback (169.254.x.y), fixed IP (IPv4)
- **Sustained Streaming speed**: DN2.20, DN2.46, DN2.47, DN2.49, DN2.59, DN2.60, DN2.61 up to 70 MByte/s, DN6.46, DN6.49 up to 100 MByte/s, DN2.59, DN2.65, DN2.22, DN2.44, DN2.66 up to 100 MByte/s, DN6.59, DN6.65, DN6.22, DN6.44, DN6.66

Power connection details

- **Power consumption**: 230 VAC, 12 VDC, 24 VDC

Serial connection details (DN2.xxx with hardware ≥ V11)

- **Serial connection (RS232)**: For diagnostic purposes only. Do not use, unless being instructed by a Spectrum support agent.

Certification, Compliance, Warranty

- **EMC Immunity**: Compliant with CE Mark
- **EMC Emission**: Compliant with CE Mark
- **Product warranty**: 5 years starting with the day of delivery
- **Software and firmware updates**: Lifetime, free of charge

DN2 specific Technical Data

Environmental and Physical Details DN2.xxx

- **Dimension of Chassis without connectors or bumpers L x W x H**: 366 mm x 267 mm x 87 mm
- **Dimension of Chassis with 19" rack mount option L x W x H**: 366 mm x 482.6 mm x 87 mm (2U height)
- **Weight (1 internal acquisition/generation module)**: 6.3 kg, with rack mount kit: 6.8 kg
- **Weight (2 internal acquisition/generation modules)**: 6.7 kg, with rack mount kit 7.2 kg
- **Warm up time**: 20 minutes
- **Operating temperature**: 0°C to 40°C
- **Storage temperature**: -10°C to 70°C
- **Humidity**: 10% to 90%
- **Dimension of packing (single DN2) L x W x H**: 470 mm x 390 mm x 180 mm
- **Volume weight of Packing (single DN2)**: 7.0 kgs

Power Consumption

- **2 + 2 channel versions**
- **4 + 4 channel versions**
- **8 + 8 channel versions**

MTBF

MTBF: TBD
Block diagram of hybridNETBOX DN2

Block diagram of Digitizer Module hybridNETBOX DN2.82x
Block diagram of AWG Module hybridNETBOX DN2./82x
Order Information

The hybridNETBOX is equipped with a large internal memory for data storage and data replay. The internal digitizer supports standard acquisition (Scope), FIFO acquisition (streaming), Multiple Recording, Gated Sampling, ABA mode and Timestamps. The internal AWG supports standard replay, FIFO replay (streaming), Multiple Replay, Gated Replay, Continuous Replay (Loop), Single-Restart as well as Sequence. Operating system drivers for Windows/Linux 32 bit and 64 bit, drivers and examples for C/C++, IVI (Scope, Digitizer and Function Generator class), LabVIEW (Windows), MATLAB (Windows and Linux), .NET, Delphi, Java, Python and a Professional license of the oscilloscope software SBench 6 are included.

The system is delivered with a connection cable meeting your country’s power connection. Additional power connections with other standards are available as option.

**hybridNETBOX DN2 - Ethernet/LXI Interface**

<table>
<thead>
<tr>
<th>Order no.</th>
<th>Memory</th>
<th>AWG</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Resolution</td>
<td>Speed</td>
</tr>
<tr>
<td>DN2.822-02</td>
<td>2 x 2 GSamples</td>
<td>16 Bit 2 x 250 MS/s</td>
</tr>
<tr>
<td>DN2.822-04</td>
<td>2 x 2 GSamples</td>
<td>16 Bit 4 x 250 MS/s</td>
</tr>
<tr>
<td>DN2.825-02</td>
<td>2 x 2 GSamples</td>
<td>14 Bit 2 x 500 MS/s</td>
</tr>
<tr>
<td>DN2.825-04</td>
<td>2 x 2 GSamples</td>
<td>14 Bit 4 x 500 MS/s</td>
</tr>
<tr>
<td>DN2.827-02</td>
<td>2 x 2 GSamples</td>
<td>16 Bit 2 x 1.25 GS/s 2 x 2.5 V</td>
</tr>
<tr>
<td>DN2.827-04</td>
<td>2 x 2 GSamples</td>
<td>16 Bit 4 x 1.25 GS/s 4 x 2.5 V</td>
</tr>
<tr>
<td>DN2.828-02</td>
<td>2 x 2 GSamples</td>
<td>14 Bit 2 x 400 MS/s</td>
</tr>
<tr>
<td>DN2.828-04</td>
<td>2 x 2 GSamples</td>
<td>14 Bit 4 x 400 MS/s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Options</th>
<th>Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>DN2.xxx-Rack</td>
<td>19&quot; rack mounting set for self-mounting</td>
</tr>
<tr>
<td>DN2.xxx-Emb</td>
<td>Extension to Embedded Server: CPU, more memory, SSD. Access via remote Linux secure shell (ssh)</td>
</tr>
<tr>
<td>DN2.xxx-spavg</td>
<td>Signal Processing Firmware Option: Block Average (later installation by firmware - upgrade available)</td>
</tr>
<tr>
<td>DN2.xxx-spstat</td>
<td>Signal Processing Firmware Option: Block Statistics/Peak Detect (later installation by firmware - upgrade available)</td>
</tr>
<tr>
<td>DN2.xxx-DC12</td>
<td>12 VDC internal power supply. Replaces AC power supply. Accepts 9 V to 18 V DC input. Screw terminals.</td>
</tr>
<tr>
<td>DN2.xxx-DC24</td>
<td>24 VDC internal power supply. Replaces AC power supply. Accepts 18 V to 36 V DC input. Screw terminals</td>
</tr>
<tr>
<td>DN2.xxx-BTPWR</td>
<td>Boot on Power On: the digitizerNETBOX/generatorNETBOX automatically boots if power is switched on.</td>
</tr>
</tbody>
</table>

**Services**

Recalibration of complete digitizerNETBOX/generatorNETBOX DN2 including calibration protocol.

**BNC Cables**

The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz.

### Technical changes and printing errors possible

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