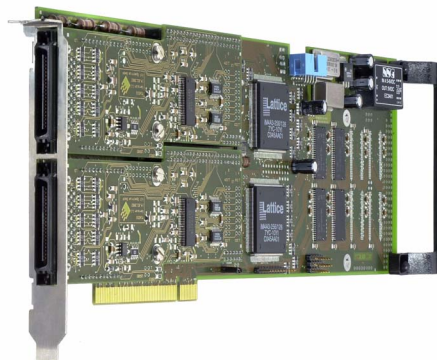


MI.70xx - 64 bit fast Digital I/O with TTL levels

- Standard PCI format
- 1, 2, 4, 8, 16 bit, 32 bit or 64 bit digital I/O
- 1 kS/s up to 125 MS/s at 16 and 32 bit
- 1 kS/s up to 60 MS/s at 32 and 64 bit
- 110 Ohm input impedance selectable
- Inputs 3.3 V and 5 V TTL compatible
- Outputs 3.3 V TTL compatible
- Up to 512 MByte memory
- FIFO mode for input and output
- Pattern/Edge/Pulsewidth trigger
- Synchronization possible
- Software SBench for Windows included
- Software SBench for Linux included



Hardware block diagram

Product range overview

Model	1-4 bit	8 bit	16 bit	32 bit	64 bit
MI.7005	125 MS/s	125 MS/s	125 MS/s		
MI.7010		125 MS/s	125 MS/s		
MI.7011		125 MS/s	125 MS/s	60 MS/s	
MI.7020		125 MS/s	125 MS/s	125 MS/s	
MI.7021		125 MS/s	125 MS/s	125 MS/s	60 MS/s

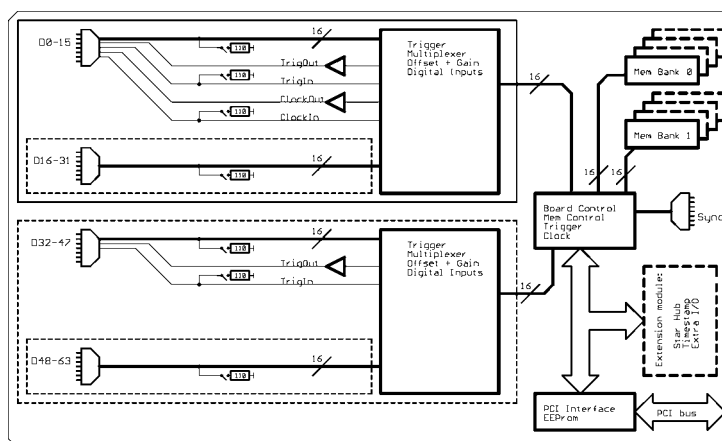
Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows NT/2000 32 bit drivers
- Windows XP/Vista/7/8/10, 32 and 64 bit driver
- Linux 32bit and 64bit drivers
- SBench 6.x Base version for Windows and Linux (recording only)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic & Excel examples
- Python examples
- LabWindows/CVI examples
- LabVIEW - drivers and examples
- MATLAB - drivers and examples
- Other 3rd party drivers (e.g. VEE, DASYLab) are partly available upon request

General Information

The MI.70xx series of fast digital I/O boards offer a resolution between 1 bit and 64 bit with a maximum sampling rate of 125 MS/s (60 MS/s). Every 16 bit / 32 bit of the board can be separately programmed for input or output. The on-board memory of up to 512 MByte can be used completely for recording or re-playing digital data. Alternatively the MI.70xx can be used in FIFO mode. Then data is transferred on-line to PC memory or hard disk. The internal standard synchronisation bus allows synchronisation of several MI.xxxx boards. Therefore the MI.70xx board can be used as an enlargement to analogue boards.



Software programmable parameters

sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Direction	Input/Output for each module
Input impedance	110 Ohm / 50 kOhm for each channel
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Trigger pulsewidth	1 to 256 samples in steps of 1
Trigger mode	Pattern and mask, edge, external TTL, software
Pattern and mask	32 bit / 64 bit wide: 0 pattern, 1 pattern, don't care or edge
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

Semiconductor test	Production test	Pattern generator
A/D data acquisition	Logic analyser	Pattern recognition

Possibilities and options

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Pattern trigger

For every bit of the digital input the pattern trigger defines individually the expected level or sets the bit to „don't care“. In combination with pulsewidth counter and edge detection the pattern trigger could be used to recognise a huge variety of trigger events.

External trigger I/O

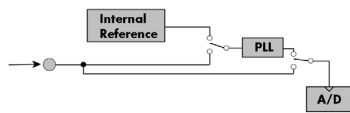
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock

The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.



The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality

Cascading

The cascading option synchronises up to 4 Spectrum boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

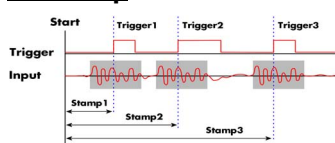
Star-Hub

The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

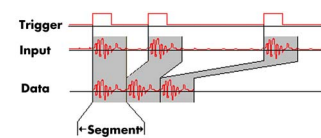
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



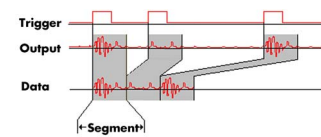
The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B or a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

Multiple Recording



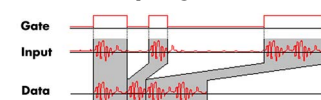
The Multiple Recording mode allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Multiple Replay



The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

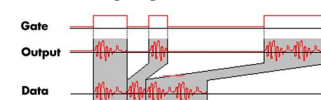
Gated Sampling



The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

programmed level.

Gated Replay



The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a

programmed level.

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Continuous output

When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

1-4 bits mode

On the model 7005 it is also possible to use just 1, 2 or 4 bits for acquisition or replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the recording/replay time in on-board memory and it reduces the transfer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times higher.

Technical Datal

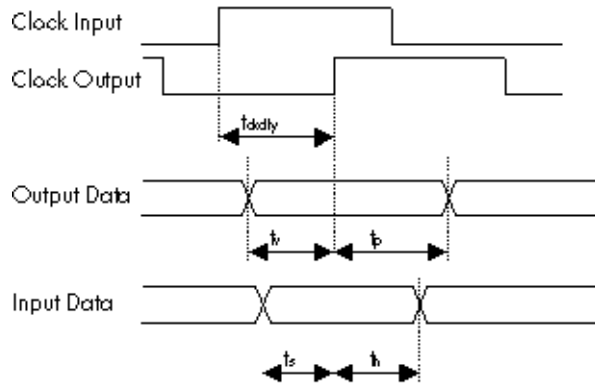
Internal samplerate	1 kS/s up to 125 MS/s			Dimension	312 mm x 107 mm		
External samplerate	DC up to 125 MS/s			Width (MI.7005, MI.701x, MI.7020)	1 full size slot		
Input impedance	110 Ohm / 50 kOhm 15 pF			Width (MI.7021)	1 full size slot and 1 half size slot		
110 Ohm termination voltage	2.5V			Connector	40 pole half pitch (Hirose FX2 series)		
Signal level (data, trigger, clock)	3.3 V/ 5 V TTL compatible			Operating temperature	0°C to 50°C		
Data input current sink (no termination)	0.0 V	3.3 V	5.0 V	Storage temperature	-10°C to 70°C		
	-1.0 µA	+1.0 µA	+20.0 µA	Humidity	10% to 90%		
Clock / trigger input current sink (no termination)	± 1.0 µA			Trigger output delay			
Multi: Trigger to 1st sample delay	fixed						
Multi: Recovery time	< 20 samples (16 - 64 bit)						
	64 bit	32 bit	16 bit	8 bit	4 bit	2 bit	1 bit
ext. Trigger accuracy (samples)	1	1	1	2	4	8	16
int. Trigger accuracy (samples)	1	1	1	2	4	8	16
Trigger input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.			Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%		
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger			Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)		

Power consumption (maximum value)	Full speed				Power down mode			
	+3,3 V	+5 V	+12 V	-12 V	+3,3 V	+5 V	+12 V	-12 V
MI.7005 (16 bit output @ 125 MS/s in 110 Ohm)	0 A	3.5 A (17.5 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A
MI.7010 (16 bit output @ 125 MS/s in 110 Ohm)	0 A	3.5 A (17.5 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A
MI.7011 (32 bit output @ 60 MS/s in 110 Ohm)	0 A	3.0 A (15.0 W)	0 A	0 A	0 A	1.5 A (7.5 W)	0 A	0 A
MI.7020 (32 bit output @ 125 MS/s in 110 Ohm)	0 A	4.9 A (24.5 W)	0 A	0 A	0 A	2.0 A (10.0 W)	0 A	0 A
MI.7021 (64 bit output @ 60 MS/s in 110 Ohm)	0 A	4.0 A (20.0 W)	0 A	0 A	0 A	2.0 A (10.0 W)	0 A	0 A

Timing of data in relation to clock

For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the 70xx series.

Delay time	External Clocking Mode		
	SINGLE	BURST S	BURST M
t_{ckdly}	20 ns	30 ns	< 1 ns
t_v	> 350 ns	> 150 ns	> 2.5 ns
t_p	> 2.5 ns	> 2.5 ns	> 2.5 ns
t_s	≤ 3.0 ns	≤ 3.0 ns	≤ 3.0 ns
t_{vh}	≤ 1.0 ns	≤ 1.0 ns	≤ 1.0 ns



Order information

Order No	Description	Order No	Description
MI7005	MI.7005 with 16 MByte (128 MBit) memory, cables and drivers	MI7xxx-32M	Option: 32 MByte memory instead of 16 MByte standard mem
MI7010	MI.7010 with 16 MByte (128 MBit) memory, cables and drivers	MI7xxx-64M	Option: 64 MByte memory instead of 16 MByte standard mem
MI7011	MI.7011 with 16 MByte (128 MBit) memory, cables and drivers	MI7xxx-128M	Option: 128 MByte memory instead of 16 MByte standard mem
MI7020	MI.7020 with 16 MByte (128 MBit) memory, cables and drivers	MI7xxx-256M	Option: 256 MByte memory instead of 16 MByte standard mem
MI7021	MI.7021 with 16 MByte (128 MBit) memory, cables and drivers	MI7xxx-512M	Option: 512 MByte memory instead of 16 MByte standard mem
MI7xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	MI7xxx-up	Additional handling cost for later memory upgrade
MI7xxx-time	Timestamp option: Extra memory for trigger time	MI7xxx-mr	Option Multiple Recording/Replay: Memory segmentation
Mlxxxx-xio	Extra I/O, internal connector: 16 DI/O, 4 Analog out	MI7xxx-gs	Option Gated Sampling: Gate signal controls acquisition/replay
Mlxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	MI7xxx-cs	Synchronisation of 2 - 4 boards, one option per system
MI70xx-dl	DASYLab driver for MI.70xx series		
MI70xx-hp	VEE driver for MI.70xx series		
MI70xx-lv	LabVIEW driver for MI.70xx series	Cab-d40-ldc-100	Additional 40 pole flat ribbon cable with IDC socket connector, ca. 1 m
MATLAB	MATLAB driver for all Ml.xxxx, MC.xxxx and MX.xxxx series.	Cab-d40-d40-100	Additional 40 pole flat ribbon cable with Fx2 connector, ca. 1 m

Technical changes and printing errors possible

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