MC.30xx - 12 bit transient recorder up to 200 MS/s

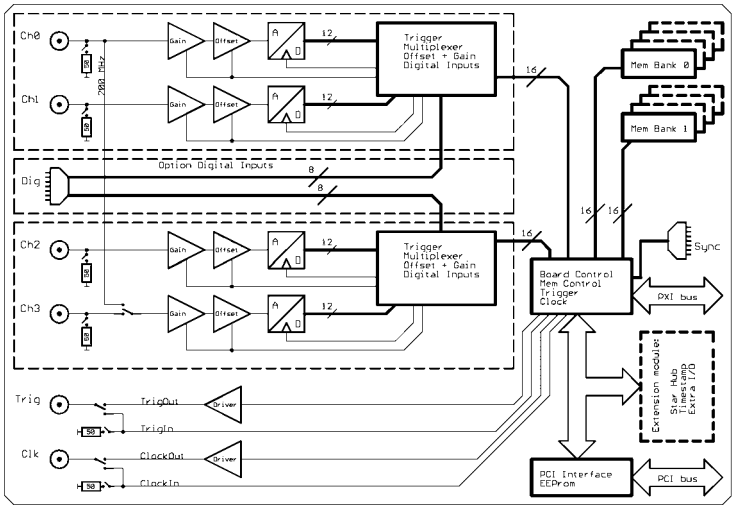
- **CompactPCI / PXI 6U format**
- **Fastest 12 bit A/D converter board**
- **Up to 200 MS/s on 1 channel**
- **Up to 100 MS/s on 2 channels**
- **Up to 60 MS/s on four channels**
- **Simultaneously sampling on all channels**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 256 MSample memory**
- **FIFO mode for slower sampling rates**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Synchronization possible**

Product range overview

All 16 boards of the MC.30xx series may use the on-board memory completely for the currently active number of channels.

Model	1 channel	2 channels	4 channels
MC.3010	80 MS/s		
MC.3011	40 MS/s	40 MS/s	
MC.3012	80 MS/s	40 MS/s	
MC.3013	40 MS/s	40 MS/s	40 MS/s
MC.3014	80 MS/s	80 MS/s	40 MS/s
MC.3015	160 MS/s	80 MS/s	
MC.3016	160 MS/s	80 MS/s	40 MS/s
MC.3020	100 MS/s		
MC.3021	50 MS/s	50 MS/s	
MC.3022	100 MS/s	50 MS/s	
MC.3023	50 MS/s	50 MS/s	50 MS/s
MC.3024	100 MS/s	100 MS/s	50 MS/s
MC.3025	200 MS/s	100 MS/s	
MC.3026	200 MS/s	100 MS/s	50 MS/s
MC.3027	100 MS/s	100 MS/s	
MC.3031	60 MS/s	60 MS/s	
MC.3033	60 MS/s	60 MS/s	60 MS/s

Hardware block diagram



Software/Drivers

A large number of drivers and examples are delivered with the board:

- Windows NT/2000 32 bit drivers
- Windows XP/Vista/7/8/10, 32 and 64 bit driver
- Linux 32bit and 64bit drivers
- SBench 6.x Base version for Windows and Linux
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic & Excel examples
- Python examples
- LabWindows/CVI examples
- LabVIEW - drivers and examples
- MATLAB - drivers and examples
- Other 3rd party drivers (e.g. VEE,DASYLab) are partly available upon request

Software programmable parameters

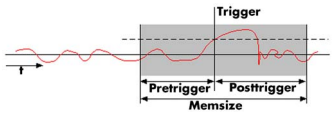
sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input Range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopie	Test of mobile communication
Ultrasound	Medical equipment	

Possibilities and options

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope instruments. Digitized data is continuously written into a ring memory until a trigger event is detected. After the trigger, post-trigger samples are recorded and pre-trigger samples can also be stored. The number of pre-trigger samples available simply equals the total ring memory size minus the number of post trigger samples.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

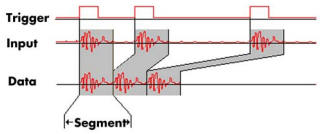
External trigger I/O

All instruments can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

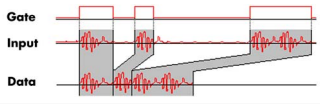
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording mode allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

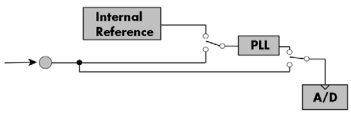


The Gated Sampling mode allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

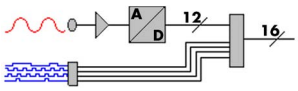
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Cascading

The cascading option synchronises up to 4 Spectrum boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

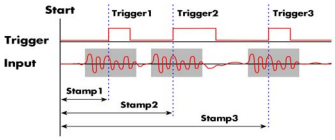
Star-Hub

The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

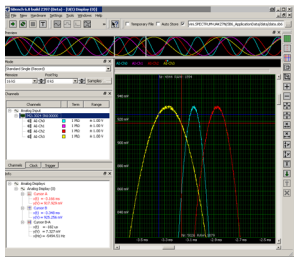
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



The timestamp function writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronized to a radio clock, an IRIG-B a GPS receiver. Using the external synchronization gives a precise time relation for acquisitions of systems on different locations.

SBench 6



A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, display acquired data and make some basic measurements. It's a valuable tool for checking the card's performance and assisting with the unit's initial setup. The cards also come with a demo license for the SBench 6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all acquisition modes including data streaming. Data streaming allows the cards to continuously acquire data and transfer it directly to the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE, GNOME and Unity) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the pro-

fessional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Technical Data

Resolution	12 bit	Input signal with 50 Ohm termination	max 5 V rms
Differential linearity error	≤ 1 LSB (ADC)	Input impedance	50 Ohm / 1 MOhm || 25 pF
Integral linearity error	≤ 1 LSB (ADC)	Overvoltage protection (range ≤ ±1 V)	±5 V
Offset error	adjustable by user	Overvoltage protection (range > ±1 V)	±50 V
Gain error	< 1%	Digital Inputs input impedance	110 Ohm @ 2.5 V
Crosstalk 1 MHz signal, 50 Ohm term	< -70 dB	Digital Inputs delay to analog sample	-12 samples
Multi: Trigger to 1st sample delay	-10 to +20 samples (fix)	Dimension	160 mm x 233 mm (6U standard)
Multi: Recovery time	< 20 samples	Width (Standard)	1 slot
ext. Trigger accuracy (<125 MS/s)	1 Samples	Width (with digital inputs or star hub)	2 slots
ext. Trigger accuracy (>160 MS/s)	2 Samples	Connector	3 mm SMB male
int. Trigger accuracy	1 Sample	Warm up time	10 minutes
Trigger output delay		Operating temperature	0°C to 50°C
Ext. clock: delay to internal clock	42 ns ± 2 ns	Storage temperature	-10°C to 70°C
Min internal clock	1 kS/s	Humidity	10% to 90%
		MTBF	100000 hours
Min external clock	1 MS/s	Power consumption 3.3 V @ full speed	max. 1.53 A (5.1 Watt)
		Power consumption 5 V @ full speed	max. 1.75 A (8.8 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	MC.3011 MC.3013	MC.3021 MC.3023	MC.3031 MC.3033	MC.3010 MC.3012 MC.3014	MC.3020 MC.3022 MC.3024 MC.3027	MC.3015 MC.3016	MC.3025 MC.3026
max internal clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	160 MS/s	200 MS/s
max external clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
-3 dB bandwidth	> 20 MHz	> 25 MHz	> 30 MHz	> 40 MHz	> 40 MHz	> 40 MHz	> 40 MHz
Zero noise level (< 125 MS/s)	< 1.5 LSB rms	< 1.5 LSB rms	< 1.75 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms
Zero noise level (> 125 MS/s)	n.a.	n.a.	n.a.	n.a.	n.a.	< 3.0 LSB rms	< 3.0 LSB rms

Dynamic Parameters

	MC.3011 MC.3013	MC.3021 MC.3023	MC.3031 MC.3033	MC.3010 MC.3012 MC.3014	MC.3020 MC.3022 MC.3024 MC.3027	MC.3015 MC.3016	MC.3025 MC.3026
Test - Samplerate	40 MS/s	50 MS/s	60 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
Testsignal frequency	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 64.8 dB	> 64.8 dB	> 63.3 dB	> 64.8 dB	> 64.7 dB	> 64.8 dB	> 63.9 dB
THD (typ)	< -73.8 dB	< -73.8 dB	< -73.2 dB	< -73.8 dB	< -73.8 dB	< -73.9 dB	< -73.5 dB
SFDR (typ), excl harm.	> 77.5 dB	> 77.5 dB	> 74.3 dB	> 77.1 dB	> 76.8 dB	> 77.0 dB	> 74.3 dB
SINAD (typ)	> 64.3 dB	> 64.3 dB	> 62.9 dB	> 64.3 dB	> 64.2 dB	> 64.3 dB	> 63.4 dB
ENOB (based on SINAD)	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB	> 10.4 LSB	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

The card is delivered with 32 MSample on-board memory and supports standard mode (Scope) and FIFO mode (streaming). Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows), LabWindows/CVI, Delphi, Visual Basic, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASYLab may be available on request.

Adapter cables are not included. Please order separately!

Versions

Order no.	1 channel	2 channels	4 channels
MC.3010	80 MS/s		
MC.3011	40 MS/s	40 MS/s	
MC.3012	80 MS/s	40 MS/s	
MC.3013	40 MS/s	40 MS/s	40 MS/s
MC.3014	80 MS/s	80 MS/s	40 MS/s
MC.3015	160 MS/s	80 MS/s	
MC.3016	160 MS/s	80 MS/s	40 MS/s
MC.3020	100 MS/s		
MC.3021	50 MS/s	50 MS/s	
MC.3022	100 MS/s	50 MS/s	
MC.3023	50 MS/s	50 MS/s	50 MS/s
MC.3024	100 MS/s	100 MS/s	50 MS/s
MC.3025	200 MS/s	100 MS/s	
MC.3026	200 MS/s	100 MS/s	50 MS/s
MC.3027	100 MS/s	100 MS/s	
MC.3031	60 MS/s	60 MS/s	
MC.3033	60 MS/s	60 MS/s	60 MS/s

Memory

Order no.	Option
MC.3xxx-64M	Memory upgrade to 64 MSample (128 MB) of total memory
MC.3xxx-128M	Memory upgrade to 128 MSample (256 MB) of total memory
MC.3xxx-256M	Memory upgrade to 256 MSample (512 MB) of total memory
MC.3xxx-up	Additional fee for later memory upgrade

Options

Order no.	Option
MC.3xxx-dig	Additional synchronous digital inputs (4 per analog channel) including Cab-d40-idc-100
MC.3xxx-cs	Option Cascading: Synchronization of up to 4 cards (one option needed per system)
MC.3xxx-smod (1)	Option Star-Hub:Synchronization of up to 16 cards (one option needed per system)
MC.3xxx-time (1)	Option Timestamp: Recording of trigger timestamps in an extra memory
MC.xxxx-xmf (1)	Option Extra I/O with external connector, 24 digital I/O + 4 analog outputs. Including one cable Cab-d40-idc-100.

Cables

		Order no.					
for Connections	Length	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female	
Analog/Clock/Trigger	80 cm	Cab-3f-9m-80	Cab-3f-9f-80	Cab-3f-3mA-80	Cab-3f-3fA-80	Cab-3f-3f-80	
Analog/Clock/Trigger	200 cm	Cab-3f-9m-200	Cab-3f-9f-200	Cab-3f-3mA-200	Cab-3f-3fA-200	Cab-3f-3f-200	
Probes (short)	5 cm		Cab-3f-9f-5				
		to 2x20 pole IDC	to 40 pole FX2				
Digital signals (option)	100 cm	Cab-d40-idc-100	Cab-d40-d40-100				

Amplifiers

Order no.	Bandwidth	Connection	Input Impedance	Coupling	Amplification
SPA.1841 (2)	2 GHz	SMA	50 Ohm	AC	x100 (40 dB)
SPA.1801 (2)	2 GHz	SMA	50 Ohm	AC	x10 (20 dB)
SPA.1601 (2)	500 MHz	BNC	50 Ohm	DC	x10 (20 dB)
SPA.1412 (2)	200 MHz	BNC	1 MOhm	AC/DC	x10/x100 (20/40 dB)
SPA.1411 (2)	200 MHz	BNC	50 Ohm	AC/DC	x10/x100 (20/40 dB)
SPA.1232 (2)	10 MHz	BNC	1 MOhm	AC/DC	x100/x1000 (40/60 dB)
SPA.1231 (2)	10 MHz	BNC	50 Ohm	AC/DC	x100/x1000 (40/60 dB)
Information	External Amplifiers with one channel, BNC/SMA female connections on input and output, manually adjustable offset, manually switchable settings. An external power supply for 100 to 240 VAC is included. Please be sure to order an adapter cable matching the amplifier connector type and matching the connector type for your A/D card input.				

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

(1) : Just one of the options can be installed on a card at a time.
(2) : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible