M4x96xx-x4 - 16 bit multi-channel multi-tone DDS up to 200 MHz

- **Fast 16 bit DAC with FPGA-based DDS**
- **One, two or four channels with 625 MS/s DAC output rate**
- **DDS frequency DC up to 200 MHz**
- **Native DDS-commands: Frequency, Amplitude, Phase, Frequency Slope, Amplitude Slope, Wait for trigger, Digital outputs**
- **DDS commands can be issued with 12.8 ns spacing**
- **PXIe 3U format, 2 slots wide**
- **Output level ±80 mV to ±2.5 V into 50 Ω (±160 mV to ±5 V into high-impedance loads)**
- **Fixed trigger to output delay**
- **Huge on-board memory for 512 Million DDS commands**
- **Two trigger input/output with AND/OR functionality**

AWG Option

The AWG firmware option adds full AWG (arbitrary waveform generator) functionality to your DDS device. The AWG mode allows to replay fully arbitrary waveforms on all active channels synchronously.

After enabling this feature and loading a new firmware, different AWG modes like Single Shot, Loop, Single Restart, Multiple Replay, Gated Replay, Streaming (FIFO) or Sequence Replay mode can be used. AWG mode also allows to freely program the sampling rate and to use synchronous digital outputs.

M4x series

- PXIe x4 Gen 2 Interface
- Works with all PXIe and PXI hybrid slots
- Up to 10 Million DDS commands per second

Operating Systems

- Windows 7 (SP1), 8, 10, 11 Server 2008 R2 and newer
- Linux Kernel 3.x, 4.x, 5.x, 6.x
- Windows/Linux 32 and 64 bit

Programming Languages

- C, C++, C#, Python
- Julia, Java, VB.NET, Delphi
- IVI (AWG option only)

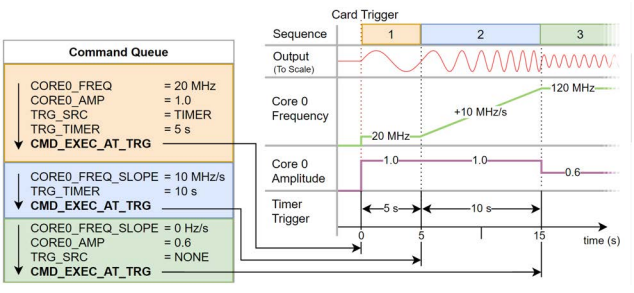
Supported Software

- SBench 6 (AWG option only)
- MATLAB
- LabVIEW

Model	Bandwidth	Channels	DDS Cores on single channel	DDS Cores on multiple channels
M4x.9621-x4	200 MHz	2	50 DDS cores	47/1 DDS cores
M4x.9622-x4	200 MHz	4	50 DDS cores	47/1/1/1 DDS cores

General Information

DDS – Direct Digital Synthesis – is a method for generating sine waves from a single, fixed-frequency reference clock and is widely used in signal generation applications. The DDS functionality implemented on Spectrum Instrumentation's AWG platform is based on the principle of adding multiple "DDS cores" to generate a multi-carrier (multi-tone) signal, with each carrier having its own well-defined frequency, amplitude and phase. In addition to these static parameters, there are also build in dynamic parameters like frequency slope and amplitude slope to allow for intrinsic linear changes for multiple cores.



**Throughput measured with a motherboard chipset supporting a TLP size of 256 bytes.

Software Support

Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8, Windows 10 and Windows 11 (32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, Delphi, Visual Basic, VB.NET, C#, Julia, Python, Java and IVI are included.

Linux Drivers

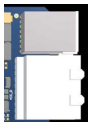
All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python and Julia, as well as the possibility to get the kernel driver sources for your own compilation.

Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW or MATLAB. All drivers come with detailed documentation and working examples are included in the delivery.

Hardware features and options

PXI Express x4



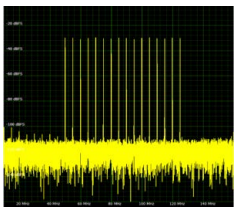
The M4x series PXI Express cards use a PCI Express x4 Gen 2 connection. They can be used in every PXI Express (PXIe) slot, as well as in any PXI hybrid slot with Gen 1, Gen 2 or Gen 3. The maximum sustained data transfer rate is more than 1.7 GByte/s (read direction) or 1.4 GByte/s (write direction) per slot.

Connections

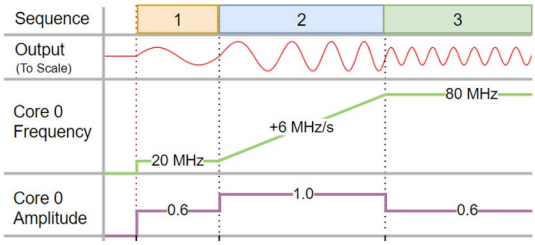
The cards are equipped with SMA connectors for the analog signals as well as for the two external trigger inputs, and clock input and output. In addition, there are three MMCX connectors that are used for the three multi-function I/O connectors. These multi-function connectors can be individually programmed to perform different functions:

- Trigger output
- Status output (armed, triggered, ready, ...)
- Synchronous digital inputs, being stored inside the analog data samples
- Asynchronous I/O lines

Multi-Tone DDS Mode



DDS - Direct Digital Synthesis - is a method for generating sine waveforms from a single, fixed-frequency reference clock and is widely used in signal generation applications. The DDS functionality implemented on Spectrum Instrumentation's AWGs is based on the principle of adding multiple "DDS cores" to generate a multi-carrier (multi-tone) signal, with each carrier having its own well-defined frequency, amplitude and phase. The right-hand frequency plot shows 16 tones. In addition to these static parameters like frequency and amplitude slope to allow for intrinsic linear changes for multiple cores.



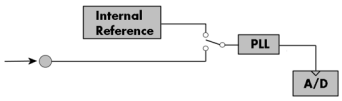
Above, the example sequence of three commands for a single core, shows a fixed 20 MHz frequency with 60% amplitude in step 1, a 10 seconds frequency ramp with 6 MHz/s slope and full 100% amplitude in step 2 and finally, in step 3, a fixed 80 MHz frequency with 50% amplitude. Each step consists of only 3 to 4 single line commands to set the mode, frequency, amplitude and timing.

Each of the cores can either be added together and output, or routed on a specific hardware output channel. A fast DMA mode allows the use of individual DDS command sequences for programming more advanced frequency changes, like shaped slopes or modulated sine signals.

External trigger input

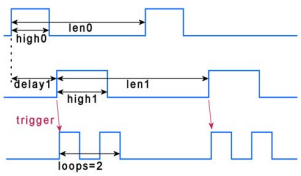
All boards can be triggered using up to two external analog or digital signals. One external trigger input has two analog comparators that can define an edge or window trigger, a hysteresis trigger or a rearm trigger. The other input has one comparator that can be used for standard edge and level triggers.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the instrument for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Firmware Option Digital Pulse Generator



The digital pulse generator option adds 4 internal independent digital pulse generators with programmable duty cycle, output frequency, delay and number of loops. These digital pulse generators can be triggered by software, hardware trigger or can trigger each other allowing to form complex pulse schemes to drive external equipment or experiments. The digital pulse generators can be output on the existing multi-XIO lines (X0, X1, ...) or can be used to trigger other pulse generators internally. Time resolution of the pulse generator depends on the cards type and the selected sampling rate and can be found in the technical data section.

The pulse generator option is a firmware option and can be later installed on all shipped cards.

Features available with the AWG firmware

option

Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

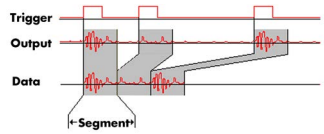
Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

FIFO mode

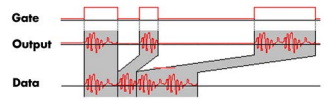
The FIFO mode is designed for continuous data transfer between PC memory or hard disk and the generation board. The control of the data stream is done automatically by the driver on an interrupt request basis. The complete installed on-board memory is used for buffering data, making the continuous streaming extremely reliable.

Multiple Replay



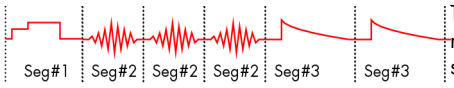
The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

Gated Replay



The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a programmed level.

Sequence Mode

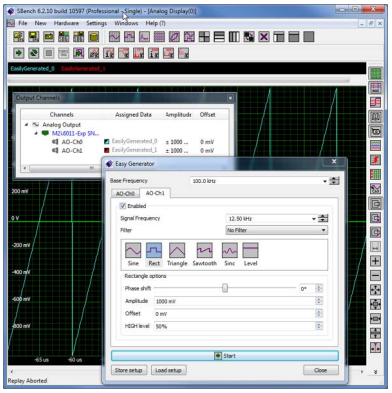


The sequence mode allows to split the card memory into several data segments of different length. These data segments are chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed. All trigger-related and software-command-related functions are only working on single cards, not on star-hub-synchrnonized cards.

External clock input and output

Using a dedicated connector a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock on a separate connector to synchronize external equipment to this clock.

SBench 6



A base license of SBench 6, the easy-to-use graphical operating software for Spectrum cards, is included in the delivery. The base license makes it is possible to test the card, generate simple signals or load and replay previously stored SBench 6 signals. It's a valuable tool for checking the cards performance and assisting with the units initial setup. The cards also come with a demo license for the SBench6 professional version. This license gives the user the opportunity to test the additional features of the professional version with their hardware. The professional version contains several advanced measurement functions, such as FFTs and X/Y display, import and export utilities as well as support for all replay modes including data streaming. Data streaming allows the cards to continuously replay data and transfer it directly from the PC RAM or hard disk. SBench 6 has been optimized to handle data files of several GBytes. SBench 6 runs under Windows as well as Linux (KDE and GNOME) operating systems. A test version of SBench 6 can be downloaded directly over the internet and can run the professional version in a simulation mode without any hardware installed. Existing customers can also request a demo license for the professional version from Spectrum. More details on SBench 6 can be found in the SBench 6 data sheet.

Technical Data

Only figures that are given with a maximum reading or with a tolerance reading are guaranteed specifications. All other figures are typical characteristics that are given for information purposes only. Figures are valid for products stored for at least 2 hours inside the specified operating temperature range, after a 30 minute warm-up, after running an on-board calibration and with proper cooled products. All figures have been measured in lab environment with an environmental temperature between 20°C and 25°C and an altitude of less than 100 m.

Analog Outputs

Resolution		16 bit		
D/A Interpolation		no interpolation		
		M4i.662x/M4x.662x DN2.662/DN6.662x DN2.82x-04 M4i.96xx/M4x.96xx DN2.96x/DN6.96x	M4i.663x/M4x.663x DN2.663/DN6.663 DN2.82x-02	
			Standard Bandwidth	With high bandwidth option (-hbw) installed
Output amplitude into 50 Ω termination	software programmable	±80 mV up to ±2.5 V	±80 mV up to ±2 V	±80 mV up to ±480 mV
Output amplitude into high impedance loads	software programmable	±160 mV up to ±5 V	±160 mV up to ±4 V	±160 mV up to ±960 mV
Stepsize of output amplitude (50 Ω termination)		1 mV	1 mV	1 mV
Stepsize of output amplitude (high impedance)		2 mV	2 mV	2 mV
10% to 90% rise/fall time of 0 V to 480 mV pulse		1.5 ns	1.1 ns	440 ps
10% to 90% rise/fall time of 0 V to 2000 mV pulse		1.5 ns	1.1 ns	n.a.

Output offset	fixed	0 V
Output Amplifier Path Selection	automatically by driver	Low Power path: ±80 mV to ±480 mV (into 50 Ω) High Power path: ±420 mV to ±2.5 V/±2 V (into 50 Ω)
Output Amplifier Setting Hysteresis	automatically by driver	420 mV to 480 mV (if output is using low power path it will switch to high power path at 480 mV. If output is using high power path it will switch to low power path at 420 mV)
Output amplifier path switching time		10 ms (output disabled while switching)
Filters	software programmable	bypass with no filter or one fixed filter
DAC Differential non linearity (DNL)	DAC only	±0.5 LSB typical
DAC Integral non linearity (INL)	DAC only	±1.0 LSB typical
Output resistance		50 Ω
Output coupling		DC
Minimum output load		0 Ω (short circuit safe)
Output accuracy	Low power path High power path	±0.5 mV ±0.1% of programmed output amplitude ±1.0 mV ±0.2% of programmed output amplitude
Offset temperature drift	after warm-up and calibration	TBD
Gain temperature drift	after warm-up and calibration	TBD
Calibration	External	External calibration calibrates the on-board references. All calibration constants are stored in non-volatile memory. A yearly external calibration is recommended.

Trigger

Available trigger modes	software programmable	External, Software, Window, Re-Arm, Or/And, Delay, PXI (M4x only)	
Trigger edge	software programmable	Rising edge, falling edge or both edges	
Trigger delay	software programmable	0 to (8GSamples - 32) = 8589934560 Samples in steps of 32 samples	
Trigger accuracy (all sources)		1 sample	
Minimum external trigger pulse width		≥ 2 samples	
External trigger		**Ext0**	**Ext1**
External trigger impedance	software programmable	50 Ω /1 kΩ	1 kΩ
External trigger coupling	software programmable	AC or DC	fixed DC
External trigger type		Window comparator	Single level comparator
External input level		±10 V (1 kΩ), ±2.5 V (50 Ω),	±10 V
External trigger sensitivity (minimum required signal swing)		2.5% of full scale range	2.5% of full scale range = 0.5 V
External trigger level	software programmable	±10 V in steps of 10 mV	±10 V in steps of 10 mV
External trigger maximum voltage		±30V	±30 V
External trigger bandwidth DC	50 Ω 1 kΩ	DC to 200 MHz DC to 150 MHz	n.a. DC to 200 MHz
External trigger bandwidth AC	50 Ω	20 kHz to 200 MHz	n.a.
Minimum external trigger pulse width		≥ 2 samples	≥ 2 samples

Clock

Clock Modes	software programmable	internal PLL, external reference clock, Star-Hub sync (generatorNETBOX and M4i only), PXI Reference Clock (M4x only)
Internal clock accuracy		≤ ±20 ppm
External reference clock range	software programmable	≥ 10 MHz and ≤ 1.25 GHz
External reference clock input impedance		50 Ω fixed
External reference clock input coupling		AC coupling
External reference clock input edge		Rising edge
External reference clock input type		Single-ended, sine wave or square wave
External reference clock input swing	square wave	0.3 V peak-peak up to 3.0 V peak-peak
External reference clock input swing	sine wave	1.0 V peak-peak up to 3.0 V peak-peak
External reference clock input max DC voltage		±30 V (with max 3.0 V difference between low and high level)
External reference clock input duty cycle requirement		45% to 55%
External reference clock output type		Single-ended, 3.3V LVPECL
Star-Hub synchronization clock modes	software selectable	Internal clock, external reference clock
Clock output		Clock output = 625 MS/s /4 = 156.25 MHz

DDS mode (50-tone DDS firmware)

Number of available DDS cores per DDS card		50
DDS core routing options	software programmable	Routed cores can individually be activated for output Ch0: 50 or 47 cores Ch1: 0 or 1 core Ch2: 0 or 1 core Ch3: 0 or 1 core
DDS commands	individual for each core	Set Frequency,, Set Amplitude, Set Phase, Frequency Slope, Amplitude Slope
DDS commands	for all cores	Reset, Execute Now, Execute at Trigger/Timer
DDS command transfer mode		single or DMA
DDS time resolution		625 MS/s (1.6 ns)
DDS timer resolution	software programmable	Preliminary: 83.2 ns up to 27.48 s with a resolution of 6.4 ns
DDS frequency range	per core programmable	0 Hz up to 625 MHz with a resolution of 0.29 Hz. Frequencies above 312.5 MHz (Nyquist-Shannon) are mirrored
DDS amplitude range	per core programmable	-1.0 up to +1.0 with a resolution of $1/(2^{32})$ programmed in relation to output level: +1.0 = 100% output, -1.0 = 100% inverted output
DDS phase range	per core programmable	-360° to +360° with a resolution of 360/4096 = 0.088°
DDS command buffer	single mode DMA mode	4k commands 512M commands in on-board RAM. More commands can reside in DMA buffer in PC-RAM.
Min user software to analog output latency	single mode DMA mode	10 us 20 us
Max continuous DDS command rate	single mode DMA mode	400 kHz 10 MHz
External trigger to DDS output change		Preliminary: ca. 1.1 us (692 samples at 1.6 ns per sample)
Maximum external re-trigger rate		72 ns (14 MHz)

Multi Purpose I/O lines (front-plate)

Number of multi purpose lines		three, named X0, X1, X2
Input: available signal types	software programmable	Asynchronous Digital-In
Input: impedance		10 kΩ to 3.3 V
Input: maximum voltage level		-0.5 V to +4.0 V
Input: signal levels		3.3 V LVTTL
Output: available signal types	software programmable	Asynchronous Digital-Out, Synchronous Digital-Out, Trigger Output, Run, Arm, Marker Output, System Clock
Output: impedance		50 Ω
Output: signal levels		3.3 V LVTTL
Output: type		3.3V LVTTL, TTL compatible for high impedance loads
Output: drive strength		Capable of driving 50 Ω loads, maximum drive strength ±48 mA
Output: update rate		sampling clock

Option M4i.xxxx-PulseGen

Number of internal pulse generators	4
Number of pulse generator output lines	3 (Existing multi-purpose outputs X0 to X2)
Time resolution of pulse generator	Pulse generator's sampling rate is derived from instrument's sampling rate and value can be read out. Maximum possible pulse generator update rate is 22xx: 156.25 MS/s (6.4 ns) 23xx: 156.25 MS/s (6.4 ns) 44xx: 125.00 MS/s (8.0 ns) 66xx: 156.25 MS/s (6.4 ns) 96xx: 156.25 MS/s (6.4 ns)
Programmable output modes	Single-shot, multiple repetitions on trigger, gated
Programmable trigger sources	Software, Card Trigger, Other Pulse Generator, XIO lines.
Programmable trigger gate	None, ARM state, RUN state
Programmable length (frequency)	2 to 4G samples in steps of 1 (32 bit)
Programmable width (duty cycle)	1 to 4G samples in steps of 1 (32 bit)
Programmable delay	0 to 4G samples in steps of 1 (32 bit)
Programmable loops	0 to 4G samples in steps of 1 (32 bit) - 0 = infinite
Output level of digital pulse generators	Please see section of multi-purpose I/O lines

Option M4i.96xx-AWG

Number of AWG options per generatorNETBOX		Each generatorNETBOX DN2.96x and DN6.96x contains multiple DDS units with either two or four channels. The user can individually decide how many of these internal DDS units should be equipped with the AWG option. Each single internal DDS unit needs a separate license.

AWG specific trigger specifications

Multi, Gate: re-arming time		40 samples
Trigger to Output Delay	sample rate ≤ 625 MS/s sample rate > 625 MS/s	238.5 sample clocks + 16 ns (valid for all modes except SPCSEQ_ENDLOOPONTRIG) 476.5 sample clocks + 16 ns (valid for all modes except SPCSEQ_ENDLOOPONTRIG)
Memory depth	software programmable	32 up to [installed memory / number of active channels] samples in steps of 32
Multiple Replay segment size	software programmable	16 up to [installed memory / 2 / active channels] samples in steps of 16

AWG specific clock specifications

Internal clock setup granularity		8 Hz (internal reference clock only, restrictions apply to external reference clock)
Setable Clock speeds		50 MHz to max sampling clock
Clock Setting Gaps		750 to 757 MHz, 1125 to 1145 MHz (no sampling clock possible in these gaps)
Clock output	sampling clock ≤71.68 MHz	Clock output = sampling clock/4
Clock output	sampling clock >71.68 MHz	Clock output = sampling clock/8

Sequence Replay Mode

Required firmware version		At least V1.14
Number of sequence steps	software programmable	1 up to 4096 (sequence steps can be overloaded at runtime)
Number of memory segments	software programmable	2 up to 64k (segment data can be overloaded at runtime)
Minimum segment size	software programmable	384 samples (1 active channel), 192 samples (2 active channels), 96 samples (4 active channels), in steps of 32 samples.
Maximum segment size	software programmable	2 GS / active channels / number of sequence segments (round up to the next power of two)
Loop Count	software programmable	1 to (1M - 1) loops
Sequence Step Commands	software programmable	Loop for #Loops, Next, Loop until Trigger, End Sequence
Special Commands	software programmable	Data Overload at runtime, sequence steps overload at runtime, readout current replayed sequence step
Limitations for synchronized products		Software commands changing the sequence as well as „Loop until trigger" are not synchronized between cards. This also applies to multiple AWG modules in a generatorNETBOX.

Bandwidth and Slewrate

	Filter	**Output Amplitude**	**663 models** (M4i.663x-x8, M4x.663x-x4, DN2.663-xx, DN6.663-xx, DN2.82x-02)	**662 and 962 models** (M4i.662x-x8, M4x.662x-x4, DN2.662-xx, DN6.662-xx, DN2.82x-04, M4i.96xx-x8, M4x.96xx-x4, DN2.96x-xx, DN6.96x-xx)
Maximum Output Rate			1.25 GS/s	625 MS/s
-3dB Bandwidth	no Filter	±480 mV	400 MHz	200 MHz
-3dB Bandwidth	no Filter	±1000 mV	320 MHz	200 MHz
-3dB Bandwidth	no Filter	±2000 mV	320 MHz	200 MHz
-3dB Bandwidth	Filter	all	65 MHz	65 MHz
Slewrate	no Filter	±480 mV	4.5 V/ns	2.25 V/ns

Dynamic Parameters

662 and 962 models
(M4i.662x-x8, M4x.662x-x4, DN2.662-xx, DN6.662-xx, DN2.82x-04, M4i.96xx-x8, M4x.96xx-x4, DN2.96x-xx, DN6.96x-xx)

Test - Samplerate	625 MS/s			625 MS/s		625 MS/s	
Output Frequency	10 MHz			50 MHz		50 MHz	
Output Level in 50 Ω	±480 mV	±1000mV	±2500mV	±480 mV	±2500mV	±480 mV	±2500mV
Used Filter	none			none		Filter enabled	
NSD (typ)	-150 dBm/Hz	-149 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz
SNR (typ)	70.7 dB	72.4 dB	63.1 dB	65.3 dB	64.4 dB	67.5 dB	69.4 dB
THD (typ)	-73.3 dB	-70.5 dB	-49.7 dB	-64.1 dB	-39.1 dB	-68.4 dB	-50.4 dB
SINAD (typ)	69.0 dB	67.7 dB	49.5 dB	61.6 dB	39.1 dB	64.9 dB	50.3 dB
SFDR (typ), excl harm.	98 dB	98 dB	99 dB	86 dB	76 dB	88 dB	89 dB
ENOB (SINAD)	11.2	11.0	8.0	10.0	6.2	10.5	8.1
ENOB (SNR)	11.5	11.7	10.2	10.5	10.4	10.9	11.2

663 models
(M4i.663x-x8, M4x.663x-x4, DN2.663-xx, DN6.663-xx, DN2.82x-02)

Test - Samplerate	1.25 GS/s			1.25 GS/s		1.25 GS/s	
Output Frequency	10 MHz			50 MHz		50 MHz	
Output Level in 50 Ω	±480 mV	±1000mV	±2000mV	±480 mV	±2000mV	±480 mV	±2000mV
Used Filter	none			none		Filter enabled	
NSD (typ)	-150 dBm/Hz	-149 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz	-150 dBm/Hz	-149 dBm/Hz
SNR (typ)	70.5 dB	72.1 dB	71.4 dB	65.2 dB	65.0 dB	67.2 dB	68.2 dB
THD (typ)	-74.5 dB	-73.5 dB	-59.1 dB	-60.9 dB	-43.9 dB	-67.9 dB	-63.1 dB
SINAD (typ)	69.3 dB	69.7 dB	59 dB	59.5 dB	43.9 dB	64.5 dB	61.9 dB

	663 models (M4i.663x-x8, M4x.663x-x4, DN2.663-xx, DN6.663-xx, DN2.82x-02)						
SFDR (typ), excl harm.	96 dB	97 dB	98 dB	85 dB	84 dB	87 dB	87 dB
ENOB (SINAD)	11.2	11.2	9.5	9.6	6.9	10.4	10.0
ENOB (SNR)	11.5	11.5	11.5	10.5	10.5	10.9	11.0

THD and SFDR are measured at the given output level and 50 Ohm termination with a high resolution M3i.4860/M4i.4450-x8 data acquisition card and are calculated from the spectrum. Noise Spectral Density is measured with built-in calculation from an HP E4401B Spectrum Analyzer. All available D/A channels are activated for the tests. SNR and SFDR figures may differ depending on the quality of the used PC. NSD = Noise Spectral Density, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range.

Connectors

Analog Inputs/Analog Outputs	SMA female (one for each single-ended input)	Cable-Type: Cab-3mA-xx-xx
Trigger 0 Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Trigger 1 Input	SMA female	Cable-Type: Cab-3mA-xx-xx
Clock Output	SMA female	Cable-Type: Cab-3mA-xx-xx
Multi Purpose I/O	MMCX female (3 lines)	Cable-Type: Cab-1m-xx-xx

Connection Cycles

All connectors have an expected lifetime as specified below. Please avoid to exceed the specified connection cycles or use connector savers.

SMA connector	500 connection cycles
MMCX connector	500 connection cycles
PXIe connector	250 connection cycles

Environmental and Physical Details

Dimension (Single Card)	(PCB only)	160 mm x 100 mm (Standard 3U)
Width		2 slots
Weight (M4x.44xx series)	maximum	340 g
Weight (M4x.22xx, M4x.66xx series)	maximum	450 g
Warm up time		10 minutes
Operating temperature		0°C to 50°C
Storage temperature		-10°C to 70°C
Humidity		10% to 90%
Dimension of packing	1 or 2 cards	470 mm x 250 mm x 130 cm
Volume weight of packing	1 or 2 cards	4 kg

PXI Express specific details

PXIe slot type	4 Lanes, PCIe Gen 2 (x4 Gen2)
PXIe hybrid slot compatibility	Fully compatible
Sustained streaming mode (Card-to-System: M4x.22xx, M4x.44xx)	> 1.7 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PXIe x4 Gen2)
Sustained streaming mode (System-to-Card: M4x.66xx, M4x.96xx)	> 1.4 GB/s (measured with a chipset supporting a TLP size of 256 bytes, using PXIe x4 Gen2)

Certification, Compliance, Warranty

Conformity Declaration	EN 17050-1:2010	General Requirements
EU Directives	2014/30/EU	EMC - Electromagnetic Compatibility
	2014/35/EU	LVD - Electrical equipment designed for use within certain voltage limits
	2011/65/EU	RoHS - Restriction of the use of certain hazardous substances in electrical and electronic equipment
	2006/1907/EC	REACH - Registration, Evaluation, Authorisation and Restriction of Chemicals
	2012/19/EU	WEEE - Waste from Electrical and Electronic Equipment
Compliance Standards	EN 61010-1: 2010	Safety regulations for electrical measuring, control, regulating and laboratory devices - Part 1: General requirement
	EN 61187:1994	Electrical and electronic measuring equipment - Documentation
	EN 61326-1:2021	Electrical equipment for measurement, control and laboratory use
	EN 61326-2-1:2021	EMC requirements - Part 1: General requirements EMC requirements - Part 2-1: Particular requirements - Test configurations, operational conditions and performance criteria for sensitive test and measurement equipment for EMC unprotected applications
	EN IEC 63000:2018	Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances
Product warranty	5 years starting with the day of delivery	
Software and firmware updates	Life-time, free of charge	

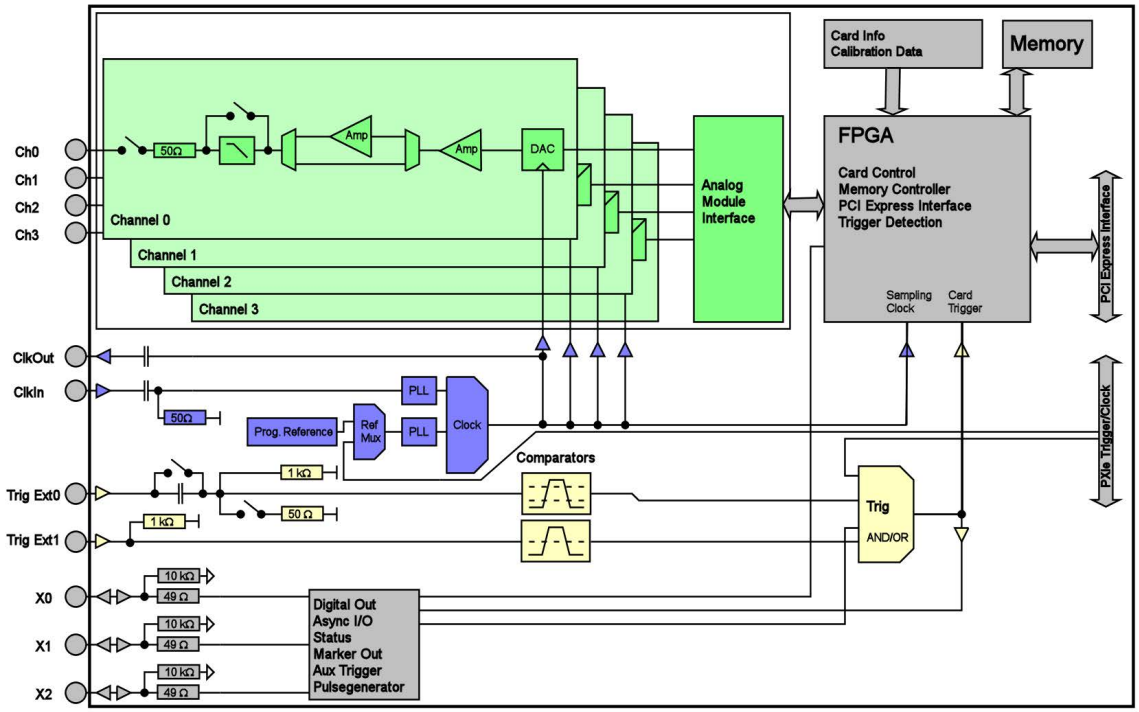
Power Consumption

		PCI EXPRESS 3.3V	12 V	Total
M4x.6620-x4	Typical values: All channels activated, Sample rate: 625 MSps	0.25 A	2.5 A	31 W
M4x.6621-x4/M4x.9621-x4	Output signal: 31.25 MHz sine wave, Output level: +/- 1 V into 50 Ω load	0.25 A	2.7 A	33 W
M4x.6622-x4/M4x.9622-x4		0.25 A	3.0 A	36 W
M4x.6620-x4/M4x.9620-x4	Typical values: All channels activated, Sample rate: 625 MSps	0.25 A	2.6 A	32 W
M4x.6621-x4/M4x.9621-x4	Output signal: 31.25 MHz sine wave, Output level: +/- 2.5 V into 50 Ω load	0.25 A	2.9 A	35 W
M4x.6622-x4/M4x.9622-x4		0.25 A	3.3 A	40 W
M4x.6630-x4	Typical values: All channels activated, Sample rate: 1.25 GSps	0.25 A	2.7 A	33 W
M4x.6631-x4	Output signal: 31.25 MHz sine wave, Output level: +/- 1 V into 50 Ω load	0.25 A	3.0 A	36 W
M4x.6630-x4	Typical values: All channels activated, Sample rate: 1.25 GSps	0.25 A	2.9 A	35 W
M4x.6631-x4	Output signal: 31.25 MHz sine wave, Output level: +/- 2.0 V into 50 Ω load	0.25 A	3.3 A	40 W

MTBF

MTBF	400.000 hours

Hardware block diagram



Order Information

The card is delivered with 4 GByte on-board memory (512 MCommands for DDS or 2 GSample for AWG data). The multi-core DDS generation is the standard mode. Adding the AWG option, the cards supports standard replay, FIFO replay (streaming), Multiple Replay, Gated Replay, Continuous Replay (Loop), Single-Restart as well as Sequence. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), IVI, .NET, Delphi, Java, Python, Julia and a Base license of the measurement software SBench 6 (AWG mode only) are included.

Adapter cables are not included. Please order separately!

PXI Express x4

Order no.	Bandwidth	DDS memory	Channels	AWG memory
M4x.9621-x4	200 MHz	512 MCommands	2	2 GSample
M4x.9622-x4	200 MHz	512 MCommands	4	2 GSample

Firmware Options

Order no.	Option
M4i.96xx-AWG	Firmware Option AWG mode. Full AWG (arbitrary waveform generator) functionality including different replay modes, freely programmable clock and trigger modes.
M4i.xxxx-PulseGen	Firmware Option: adds 4 freely programmable digital pulse generators that use the XIO lines for output (later installation by firmware -upgrade available)

Standard Cables

		Order no.				
for Connections	Length	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
Analog/Clock-In/Trig-In	80 cm	Cab-3mA-9m-80	Cab-3mA-9f-80	Cab-3mA-3mA-80		Cab-3f-3mA-80
Analog/Clock-In/Trig-In	200 cm	Cab-3mA-9m-200	Cab-3mA-9f-200	Cab-3mA-3mA-200		Cab-3f-3mA-200
Probes (short)	5 cm		Cab-3mA-9f-5			
Clk-Out/Trig-Out/Extra	80 cm	Cab-1m-9m-80	Cab-1m-9f-80	Cab-1m-3mA-80	Cab-1m-3fA-80	Cab-1m-3f-80
Clk-Out/Trig-Out/Extra	200 cm	Cab-1m-9m-200	Cab-1m-9f200	Cab-1m-3mA-200	Cab-1m-3fA-200	Cab-1m-3f-200
Information	The standard adapter cables are based on RG174 cables and have a nominal attenuation of 0.3 dB/m at 100 MHz and 0.5 dB/m at 250 MHz. For high speed signals we recommend the low loss cables series CHF					

Low Loss Cables

Order No.	Option
CHF-3mA-3mA-200	Low loss cables SMA male to SMA male 200 cm
CHF-3mA-9m-200	Low loss cables SMA male to BNC male 200 cm
Information	The low loss adapter cables are based on MF141 cables and have an attenuation of 0.3 dB/m at 500 MHz and 0.5 dB/m at 1.5 GHz. They are recommended for signal frequencies of 200 MHz and above.

Services

Order no.	
Recal	Recalibration at Spectrum incl. calibration protocol

Software SBench6

Order no.	
SBench6	Base version included in delivery. Supports standard mode for one card.
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

Software Options

Order no.	
SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p/M5i cards
SPc-SCAPP	Spectrum's CUDA Access for Parallel Processing - SDK for direct data transfer between Spectrum card and CUDA GPU. Includes RDMA activation and examples.

(1) : Just one of the options can be installed on a card at a time.
(2) : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible