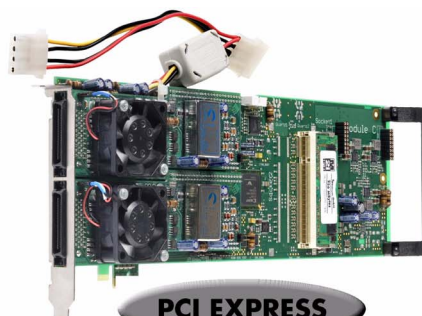


## M2i.72xx - 32 bit pattern generator with programmable levels

- Programmable output levels from -2,0 V up to +10,0 V
- Levels individually programmable per 4 bit
- Up to 40 MS/s at 32 bit
- All Outputs can be separately disabled (Tristate)
- Hardware controlled differential output possible
- Up to 2 GByte on-board memory
- 512 MByte standard memory installed
- FIFO mode for output
- Sustained streaming mode
- Edge/pulse width/delay trigger
- Synchronization of up to 16 cards per system and up to 271 cards with system sync
- Features: Multiple Replay, Gated Replay, BaseXIO



PCI / PCI-X



PCI EXPRESS

- 66 MHz 32 bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 245 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16\* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

<u>Operating Systems</u>	<u>Recommended Software</u>	<u>Drivers</u>
<ul style="list-style-type: none"> <li>• Windows 7 (SP1), 8, 10, Server 2008 R2 and newer</li> <li>• Linux Kernel 2.6, 3.x, 4.x, 5.x</li> <li>• Windows/Linux 32 and 64 bit</li> </ul>	<ul style="list-style-type: none"> <li>• Visual C++, Delphi, C++ Builder, GNU C++, VB.NET, C#, J#, Java, Python</li> <li>• SBench 6</li> </ul>	<ul style="list-style-type: none"> <li>• MATLAB</li> <li>• LabVIEW</li> </ul>

Model	1-4 bit	8 bit	16 bit	32 bit
M2i.7210	10 MS/s	10 MS/s	10 MS/s	
M2i.7211	10 MS/s	10 MS/s	10 MS/s	5 MS/s
M2i.7220	40 MS/s	40 MS/s	40 MS/s	
M2i.7221	40 MS/s	40 MS/s	40 MS/s	40 MS/s

### General Information

The M2i.72xx pattern generator series gives the user the possibility to generate digital data with a wide range of output levels. For every 4 bit the LOW and HIGH levels can be programmed from -2.0 V up to +10.0 V. Even at high speeds you are not limited concerning the maximum output swing. This enables the user to drive devices of nearly any logic family, like ECL, PECL, TTL, LVDS, LVTTTL, CMOS or LVCMOS. The potentially necessary differential signals are generated in hardware, so that only one data bit is used for each pair of differential signals. The on-board memory of up to 2 GByte can be used completely for recording or replaying digital data. Alternatively the M2i.70xx can be used in FIFO mode. Then data is transferred on-line from PC memory or hard disk. All boards of the M2i.72xx series may use the whole installed on-board memory completely for the currently activated number of channels.

\*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

## Software Support

### Windows drivers

The cards are delivered with drivers for Windows 7, Windows 8 and Windows 10 (each 32 bit and 64 bit). Programming examples for Visual C++, C++ Builder, LabWindows/CVI, Delphi, Visual Basic, VB.NET, C#, J#, Java and Python are included.

### Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like Fedora, Suse, Ubuntu LTS or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for GNU C++, Python as well as the possibility to get the driver sources for your own compilation.

### SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME).

### Third-party products

Spectrum supports the most popular third-party software products such as LabVIEW, MATLAB or LabWindows/CVI. All drivers come with detailed documentation and working examples are included in the delivery. Support for other software packages, like VEE or DasyLab, can also be provided on request.

### MI Software compatibility layer

To allow an easy change from MI cards to the new M2i cards for existing software a special software compatibility layer is delivered with the cards. This DLL converts MI calls to M2i calls and simulates a MI card in the software.

## Hardware features and options

### PCI/PCI-X



The cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in PCI-

X or PCI 64 slots. The maximum sustained data transfer rate is 245 MByte/s per bus segment.

### PCI Express



The cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maximum sustained data transfer rate is

160 MByte/s per slot.

### FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 245 MB/s on a PCI-X slot, up to 125 MB/s on a PCI slot and up to 160 MB/s on a PCIe slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-

board memory is used for buffer data, making the continuous streaming extremely reliable.

### Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

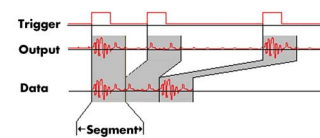
### Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

### Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

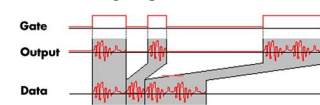
### Multiple Replay



The Multiple Replay mode allows the fast output generation on several trigger events without restarting the hardware. With this option very fast repetition rates can be

achieved. The on-board memory is divided into several segments of the same size. Each segment can contain different data which will then be played with the occurrence of each trigger event.

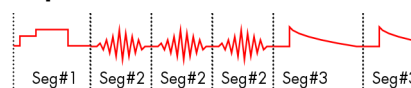
### Gated Replay



The Gated Sampling mode allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has attained a

programmed level.

### Sequence Mode



The sequence mode allows to split the card memory into several

data segments of different length. These data segments are chained up in a user chosen order using an additional sequence memory. In this sequence memory the number of loops for each segment can be programmed and trigger conditions can be defined to proceed from segment to segment. Using the sequence mode it is also possible to switch between replay waveforms by a simple software command or to redefine waveform data for segments simultaneously while other segments are being replayed. All trigger-related and software-command-related functions are only working on single cards, not on star-hub-synchronized cards.

### External trigger I/O

All digital boards can be triggered using an additional external TTL signal per acquisition module. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognized trigger event can - when activated by software - be routed to the trigger output connector to start external instruments.

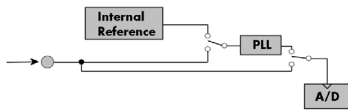
### Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

### External clock I/O

Using a dedicated line a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronize external equipment to this clock.

### Reference clock



The option to use a precise external reference clock (typically 10 MHz) is necessary to synchronize the instrument for high-quality

measurements with external equipment (like a signal source). It's also possible to enhance the stability of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

### Singleshot output

When singleshot output is activated the data of the on-board memory is played exactly one time. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

### Repeated output

When the repeated output mode is used the data of the on-board memory is played continuously for a programmed number of times or until a stop command is executed. The trigger source can be either one of the external trigger inputs or the software trigger. After the first trigger additional trigger events will be ignored.

### Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. The trigger source can be either the external TTL trigger or software trigger.

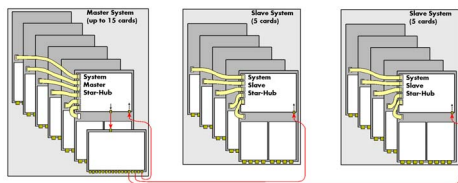
### Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and

clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

### 271 synchronous cards with the System Star-Hub



With the help of multiple system star-hubs it is possible to link up to 17 system phase synchronous with each other.

Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in a bunch of systems. One master system distributes clock and trigger signal to all connected slave systems.

### 1-4 bits mode

On all models it is also possible to use just 1, 2 or 4 bits for replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the replay time in on-board memory and it reduces the trans-

fer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times higher.

### BaseXIO (Asynchronous I/O, enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. This allows e.g. external equipment control or status monitoring. Two of these lines can also be used as additional external trigger sources. This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

## Technical Data

### Power Up

Data channels state after power up  
Clock and trigger output after power up

tristate (high impedance)  
disabled

### Digital Outputs

Output channels  
Output impedance  
Data signal level  
Programmable level accuracy  
Max output current per pin  
Max output current per nibble (4 bit)  
Max output current per card  
Rise/Fall time 10% to 90%, 110 ohm

software programmable

1, 2, 4, 8, 16 or 32  
approximately 80 Ohm  
programmable from -2.0 V up to +10.0 V  
±10 mV  
100 mA  
200 mA  
500 mA (M2i.721x cards, otherwise no limit)  
2.0 ns (1 MS/s) up to 2.25 ns (40 MS/s)

### Output Delays

Trigger to 1st sample  
Trigger to 1st sample  
Gate end to last replayed sample  
Gate end alignment

≥ 8 active channels  
< 8 active channels

18 clocks  
8 clocks + 10 \* 8/active channels  
18 samples (≥ 8 active channels)  
[32 / active channels] in samples

### Trigger

Running mode  
Trigger modes  
Trigger edge  
Trigger pulse width  
Trigger delay  
Memory depth  
Posttrigger  
Multiple Replay segment size  
Multiple Replay, Gated Replay: re-arming time  
Pretrigger at Multi, Gate, FIFO Recording  
Trigger output delay  
Internal/External trigger accuracy  
Internal/External trigger accuracy  
External trigger type (input and output)  
External trigger input  
External trigger maximum voltage  
Trigger impedance  
External trigger output levels  
External trigger maximum voltage  
External trigger input current sink  
External trigger output drive strength

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

Singleshot, FIFO mode (Streaming), Multiple Replay, Gated Replay, Repeated Replay, Single Restart, Sequence Mode  
External TTL, software, pulsewidth, Or/And, Delay  
Rising edge, falling edge or both edges  
0 to [64k - 1] samples in steps of 1 sample  
0 to [64k - 1] samples in steps of 1 sample  
8 up to [installed memory / number of active channels] samples in steps of 4  
4 up to [8G - 4] in steps of 4  
8 up to [installed memory / 2 / active channels] samples in steps of 4  
< 4 samples  
8 up to [16352 Bytes / number of active channels] in steps of 8  
19 clocks  
1 sample  
8/active channels samples (< 8 channels)  
3.3V LVTTTL compatible (5V tolerant)  
Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods  
-0.5 V up to +5.7 V (internally clamped to 5.0V, 100 mA max. clamping current)  
110 Ohm / high impedance (> 4 kΩ)  
Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible  
-0.5 V up to +5.5 V  
± 1.0 μA (no termination)  
Capable of driving 110 Ω and 50 Ω load

### Clock

Clock Modes  
Internal clock range (PLL mode)  
Internal clock accuracy  
Internal clock setup granularity  
External reference clock range  
External clock impedance  
External clock range  
External clock delay to internal clock  
External clock type/edge  
External clock input  
External clock maximum voltage  
External clock output levels  
External clock output drive strength  
External clock input current sink  
Synchronization clock divider

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

software programmable

internal PLL, internal quartz, external. clock, external divided, external reference clock, sync  
1 kS/s to max using internal reference, 50kS/s to max using external reference clock  
≤ 20 ppm  
≤ 1% of range (100M, 10M, 1M, 100k,...): Examples: range 1M to 10M: stepsize ≤ 100k  
≥ 1.0 MHz and ≤ 125.0 MHz  
110 Ω / high impedance (> 4 kΩ)  
DC up to max internal sample rate  
5.4 ns  
3.3V LVTTTL compatible, rising edge used  
Low level ≤ 0.8 V, High level ≥ 2.0 V, duty cycle: 45% - 55%  
-0.5 V up to +5.5 V (internally clamped to 5.0V, 100 mA max. clamping current)  
Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible  
Capable of driving 110 Ω and 50 Ω load  
± 1.0 μA (no termination)  
2 up to [8k - 2] in steps of 2

## **Sequence Replay Mode**

Number of sequence steps	software programmable	1 up to 512 (sequence steps can be overloaded at runtime)
Number of memory segments	software programmable	2 up to 256 (segment data can be overloaded at runtime)
Minimum segment size	software programmable	48 samples (8 active channels) in steps of 16 samples., 32 samples (16 active channels) in steps of 8 samples., 32 samples (32 active channels) in steps of 4 samples.
Maximum segment size	software programmable	Installed on-board memory (in bytes) / (1, 2, 4 or 8 for 8, 16, 32 or 64 active channels) / number of sequence segments (round up to the next power of two)
Loop Count	software programmable	1 to 1M loops
Sequence Step Commands	software programmable	Loop for #Loops, Next, Loop until Trigger, End Sequence
Special Commands	software programmable	Data Overload at runtime, sequence steps overload at runtime
Limitations for synchronized products		Software commands changing the sequence as well as „Loop until trigger“ are not synchronized between cards.

## **BaseXIO Option**

BaseXIO modes	software programmable	Asynch digital I/O, 2 additional trigger, timestamp reference clock, timestamp digital inputs
BaseXIO direction	software programmable	Each 4 lines can be programmed in direction
BaseXIO input		TTL compatible: Low $\leq$ 0.8 V, High $\geq$ 2.0 V
BaseXIO input impedance		4.7 kOhm towards 3.3 V
BaseXIO input maximum voltage		-0.5 V up to +5.5 V
BaseXIO output type		3.3 V LVTTL
BaseXIO output levels		TTL compatible: Low $\leq$ 0.4 V, High $\geq$ 2.4 V
BaseXIO output drive strength		32 mA maximum current, no 50 $\Omega$ loads

## **Connectors**

Digital Inputs/Outputs	40 pole half pitch (Hirose FX2 series)	Cable-Type: Cab-d40-xx-xx
	Connector on card: Hirose FX2B-40PA-1.27DSL	
	Flat ribbon cable connector: Hirose FX2B-40SA-1.27R	
Option BaseXIO	8 x 3 mm SMB male on extra bracket, internally 8 x MMCX female	

## **Environmental and Physical Details**

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or with option star-hub 5)	1 full size slot
Width (star-hub 16)	additionally back of adjacent neighbour slots
Width (with option BaseXIO)	additionally extra bracket on neighbour slot
Width (with option -digin, -digout or -60xx-AmpMod)	additionally half length of adjacent neighbour slot
Weight (depending on version)	290g (smallest version) up to 460g (biggest version with all options, including star-hub)
Warm up time	10 minutes
Operating temperature	0°C to 50°C
Storage temperature	-10°C to 70°C
Humidity	10% to 90%

## **PCI/PCI-X specific details**

PCI / PCI-X bus slot type	32 bit 33 MHz or 32 bit 66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3,3 V and 5 V I/O
Sustained streaming mode	> 245 MB/s (in a PCI-X slot clocked at 66 MHz or higher)

## **PCI Express specific details**

PCIe slot type	x1 Generation 1
PCIe slot compatibility (physical)	x1, x4, x8, x16
PCIe slot compatibility (electrical)	x1, x2, x4, x8, x16 with Generation 1, Generation 2, Generation 3, Generation 4
Sustained streaming mode	> 160 MB/s

## **Certification, Compliance, Warranty**

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	5 years starting with the day of delivery
Software and firmware updates	Lifetime, free of charge

## Power Consumption

	PCI / PCI-X					PCI EXPRESS			
	+3.3 V Bus	+5 V Bus	+12V Bus	+12V Cable	Total	+3.3V Bus	+12V Bus	+12V Cable	Total
M2i.7210 (512 MB memory)	1.7 A	0.5 A	0.4 A	-	12.9 W	0.4 A	1.1 A	-	14.5 W
M2i.7211 (512 MB memory)	1.8 A	0.6 A	0.4 A	-	13.8 W	0.4 A	1.2 A	-	15.7 W
M2i.7220 (512 MB memory)	1.9 A	0.1 A	-	1.5 A	24.8 W	0.4 A	0.7 A	1.5 A	27.7 W
M2i.7221 (512 MB memory)	2.3 A	0.1 A	-	3.0 A	44.1 W	0.4 A	0.8 A	3.0 A	46.9 W
M2i.7221 (4 GB memory), max. power	3.9 A	0.1 A	-	3.0 A	49.4 W	0.4 A	1.2 A	3.0 A	51.7 W

## MTBF

MTBF

200000 hours

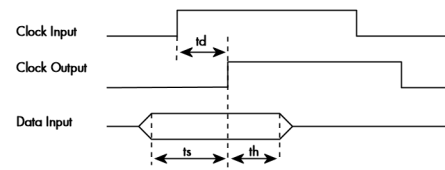
## External clock-to-data timing

The setup and hold times as well as any delays relate to the output clock. If using external clock the timing depends on the used external range. Please be sure to meet this timing constraints if feeding in external clock.

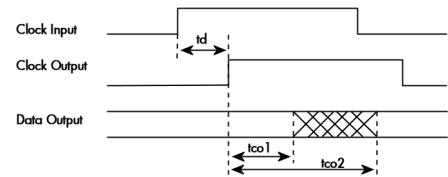
For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the M2i.72xx series.

Input	Delay time	External Clocking Mode		Internal Clocking
		EXRANGE_LOW	EXRANGE_LOW_DPS	
Data Output	$t_d$	16.9 ns	1.6 ns	n.a.
	$t_{co1}$	12 ns (typ.)	12 ns (typ.)	12 ns (typ.)
Trigger Output	$t_{co2}$	18 ns (max.)	18 ns (max.)	18 ns (max.)
	$t_{co1}$	2.2 ns	2.2 ns	2.2 ns
Trigger Input	$t_{co2}$	6.6 ns	6.6 ns	6.6 ns
	$t_s$	1.5 ns	1.5 ns	1.5 ns
	$t_h$	1.8 ns	1.8 ns	1.8 ns

### Input timing



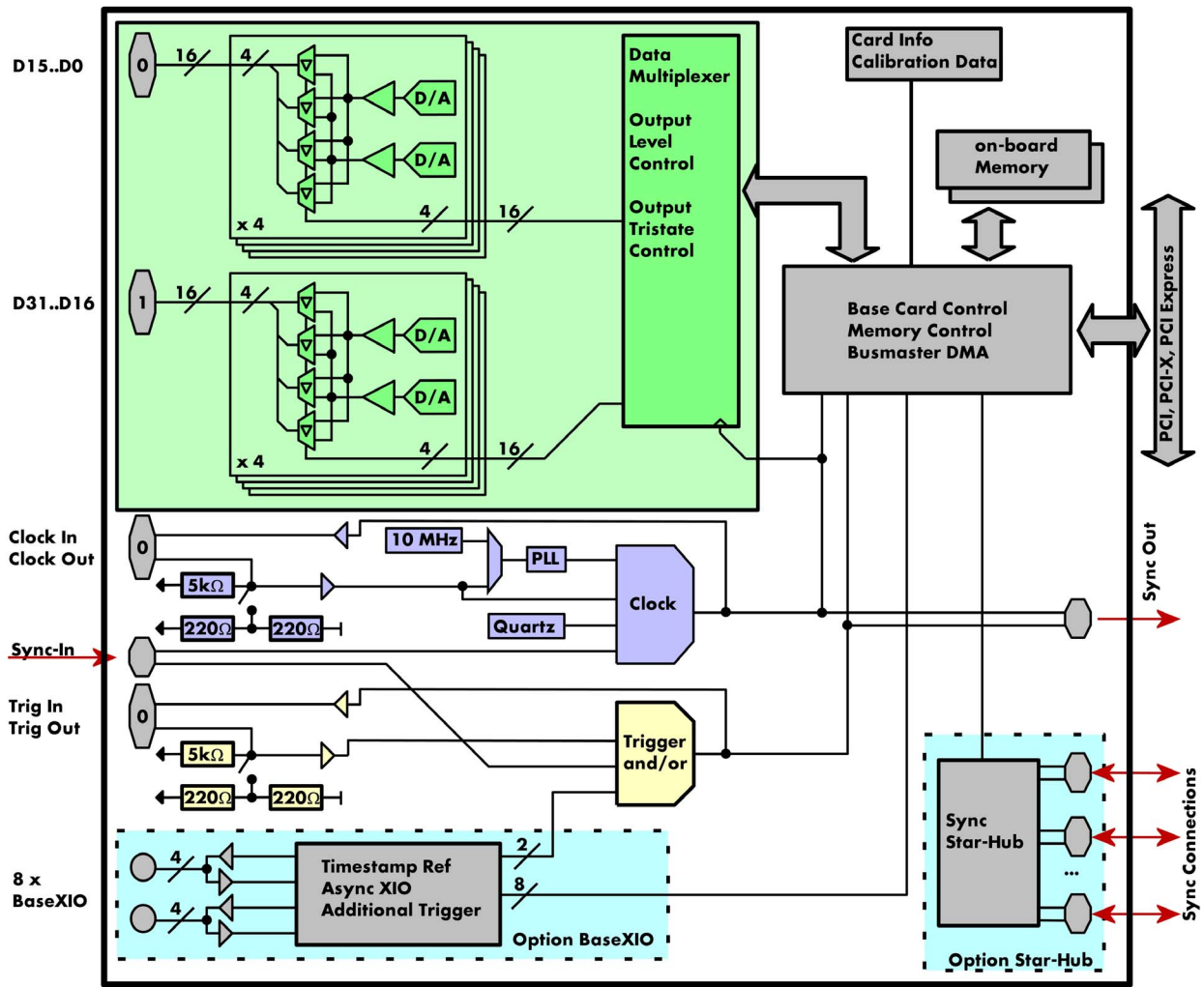
### Output timing



When using external clock a delayed clock signal is generated on the Clock Output pin.

The timing data in relation to this delayed clock output is similar to the timing when using internal clocking. It is therefore strongly recommended that you use the delay clock output for clocking any external devices.

# Hardware block diagram



## Order Information

The card is delivered with 512 MByte on-board memory and supports standard acquisition and replay (scope, single-shot, loop, single start), FIFO acquisition/replay (streaming), Multiple Recording/Replay, Gated Sampling/Replay, Timestamps and Sequence Mode. Operating system drivers for Windows/Linux 32 bit and 64 bit, examples for C/C++, LabVIEW (Windows), MATLAB (Windows and Linux), .NET, Delphi, Java, Python and a Base license of the oscilloscope software SBench 6 are included. Drivers for other 3rd party products like VEE or DASyLab may be available on request.

One digital connecting cable Cab-d40-idx-100 is included in the delivery for every digital connection (each 16 channels).

PCI Express (PCIe) PCI/PCI-X	PCI Express	PCI/PCI-X	Standard Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit
	M2i.7210-exp	M2i.7210	512 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	
	M2i.7211-exp	M2i.7211	512 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	5 MS/s
	M2i.7220-exp	M2i.7220	512 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	
	M2i.7221-exp	M2i.7221	512 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s

Memory	Order no.	Option
	M2i.xxxx-1GB	Memory upgrade to 1 GB of total memory
	M2i.xxxx-2GB	Memory upgrade to 2 GB of total memory

Options	Order no.	Option
	M2i.xxxx-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
	M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
	M2i.xxxx-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, PCI 32 Bit card, sync cables and extra bracket for clock and trigger distribution included
	M2i.xxxx-SSHMe (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, PCI Express card, sync cables and extra bracket for clock and trigger distribution included
	M2i.xxxx-SSHS5 (1)	System-Star-Hub Slave for 5 cards in one system, one slot width all sync cables + bracket included
	M2i.xxxx-SSHS16 (1)	System-Star-Hub Slave for 16 cards in system, two slots width, all sync cables + bracket included
	M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O and additional external trigger lines, additional bracket with 8 SMB connectors
	M2i-upgrade	Upgrade for M2i.xxxx: later installation of option -M2i.xxxx-2GB, -dig, -2DigM, -4DigM, -SH5, -SH16 or -bxio

Cables	for Connections	Length	Order no.	to BNC male	to BNC female	to SMA male	to SMA female	to SMB female
	BaseXIO line	80 cm		Cab-3f-9m-80	Cab-3f-9f-80	Cab-3f-3mA-80	Cab-3f-3fA-80	Cab-3f-3f80
	BaseXIO line	200 cm		Cab-3f-9m-200	Cab-3f-9f-200	Cab-3f-3mA-200	Cab-3f-3fA-200	Cab-3f-3f200
				to 2x20 pole IDC	to 40 pole FX2			
	Digital signals	100 cm		Cab-d40-idx-100	Cab-d40-d40-100			

Software SBench6	Order no.	Option
	SBench6	Base version included in delivery. Supports standard mode for one card.
	SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
	SBench6-Multi	Option multiple cards: Needs SBench6-Pro. Handles multiple synchronized cards in one system.
	Volume Licenses	Please ask Spectrum for details.

Software Options	Order no.	Option
	SPc-RServer	Remote Server Software Package - LAN remote access for M2i/M3i/M4i/M4x/M2p cards

<sup>(1)</sup> : Just one of the options can be installed on a card at a time.

<sup>(2)</sup> : Third party product with warranty differing from our export conditions. No volume rebate possible.

### Technical changes and printing errors possible

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